

GIGABYTE GA-M57SLI-S4 Schematics

Revision:2.03

SHEET

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SHEET

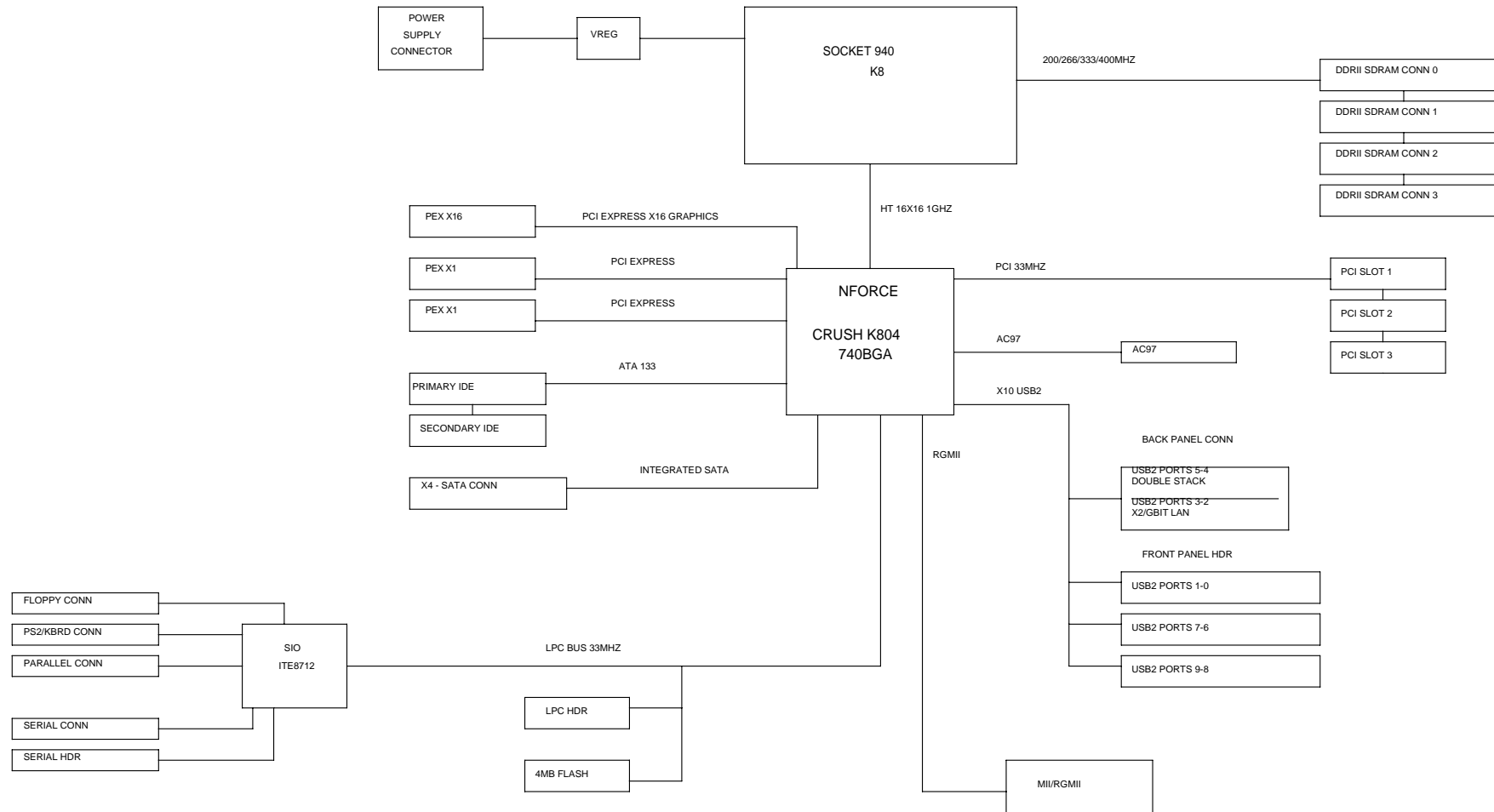
TITLE

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Title			
BLOCK DIAGRAM			
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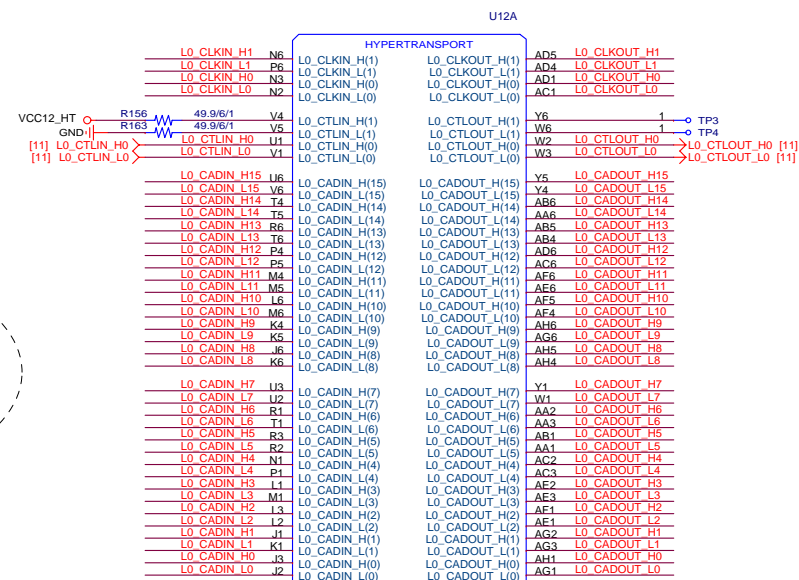
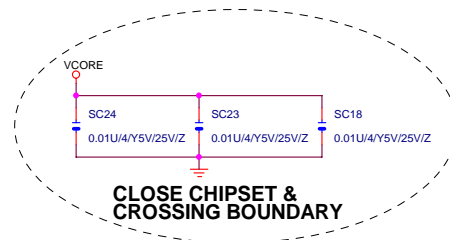
BLOCK DIAGRAM



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L0_CADIN_L0_15] <L0_CADIN_L0_15] [11]
L0_CADIN_H0_15] <L0_CADIN_H0_15] [11]
L0_CLKIN_L0_1] <L0_CLKIN_L0_1] [11]
L0_CLKIN_H0_1] <L0_CLKIN_H0_1] [11]
L0_CADOUT_L0_15] <L0_CADOUT_L0_15] [11]
L0_CADOUT_H0_15] <L0_CADOUT_H0_15] [11]
L0_CLKOUT_L0_1] <L0_CLKOUT_L0_1] [11]
L0_CLKOUT_H0_1] <L0_CLKOUT_H0_1] [11]

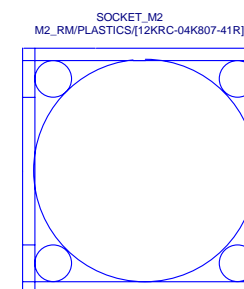


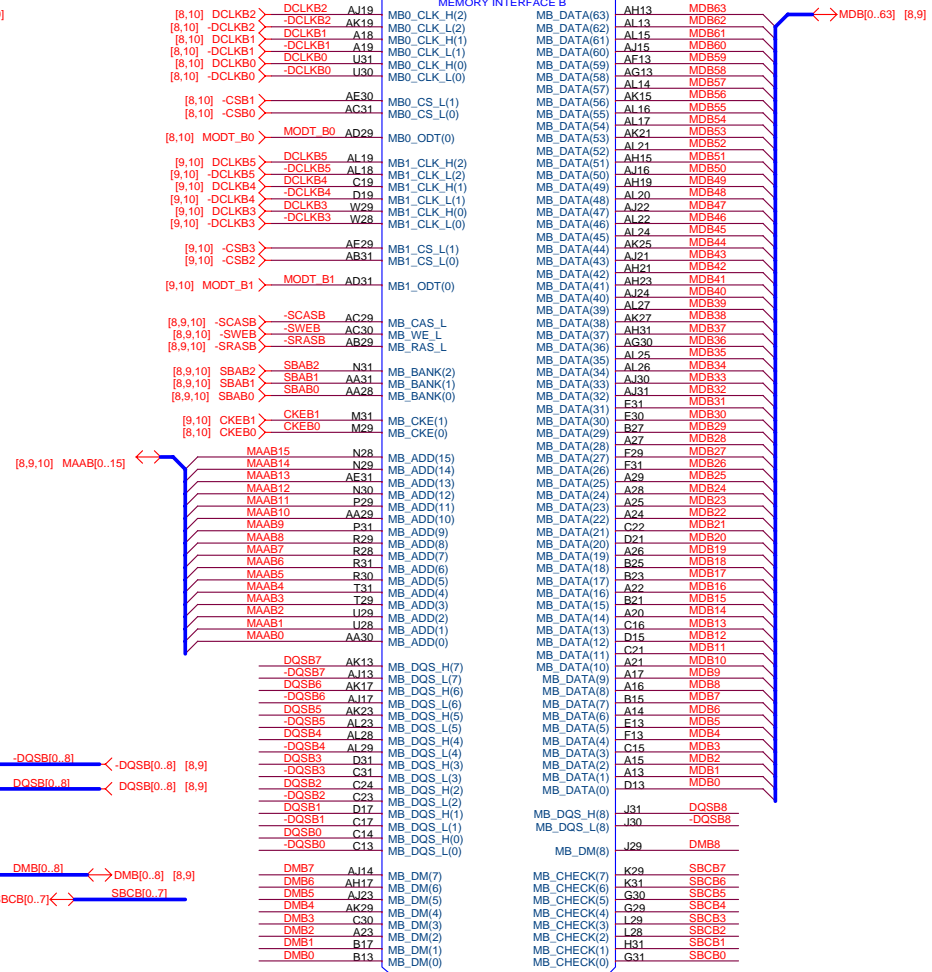
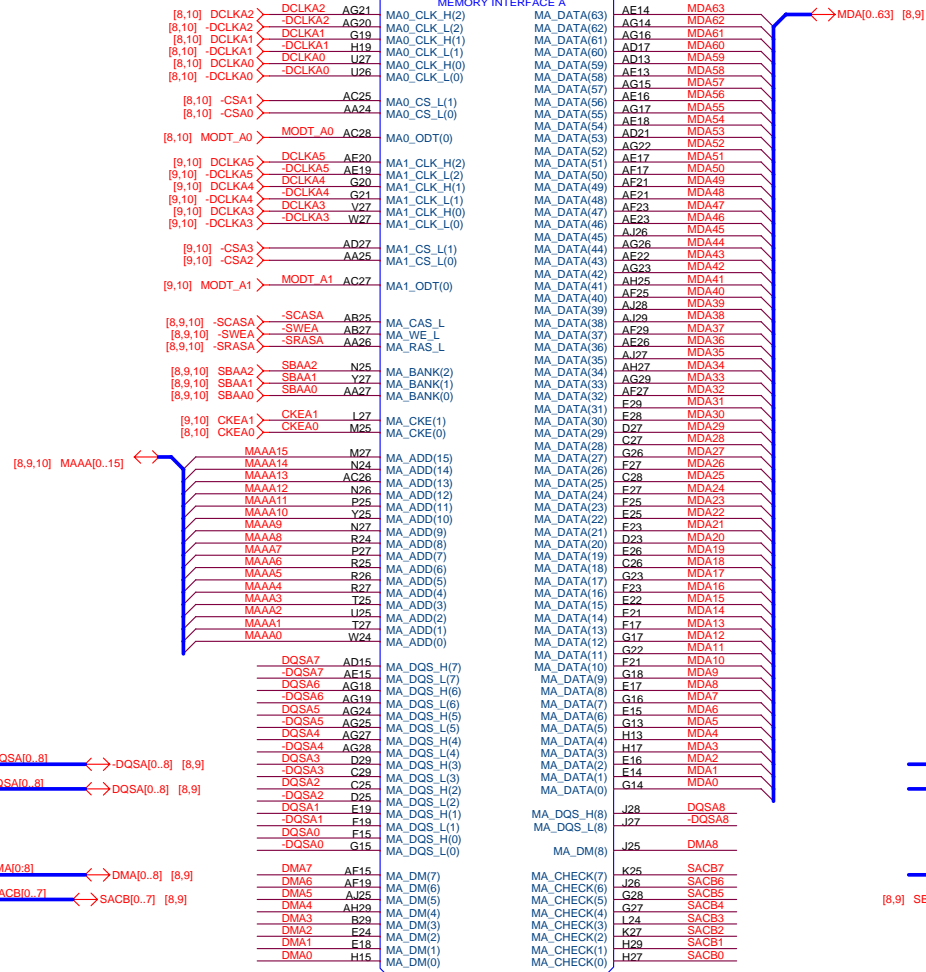
```
CPU_VDDA_RUN = VDDA25
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT
```

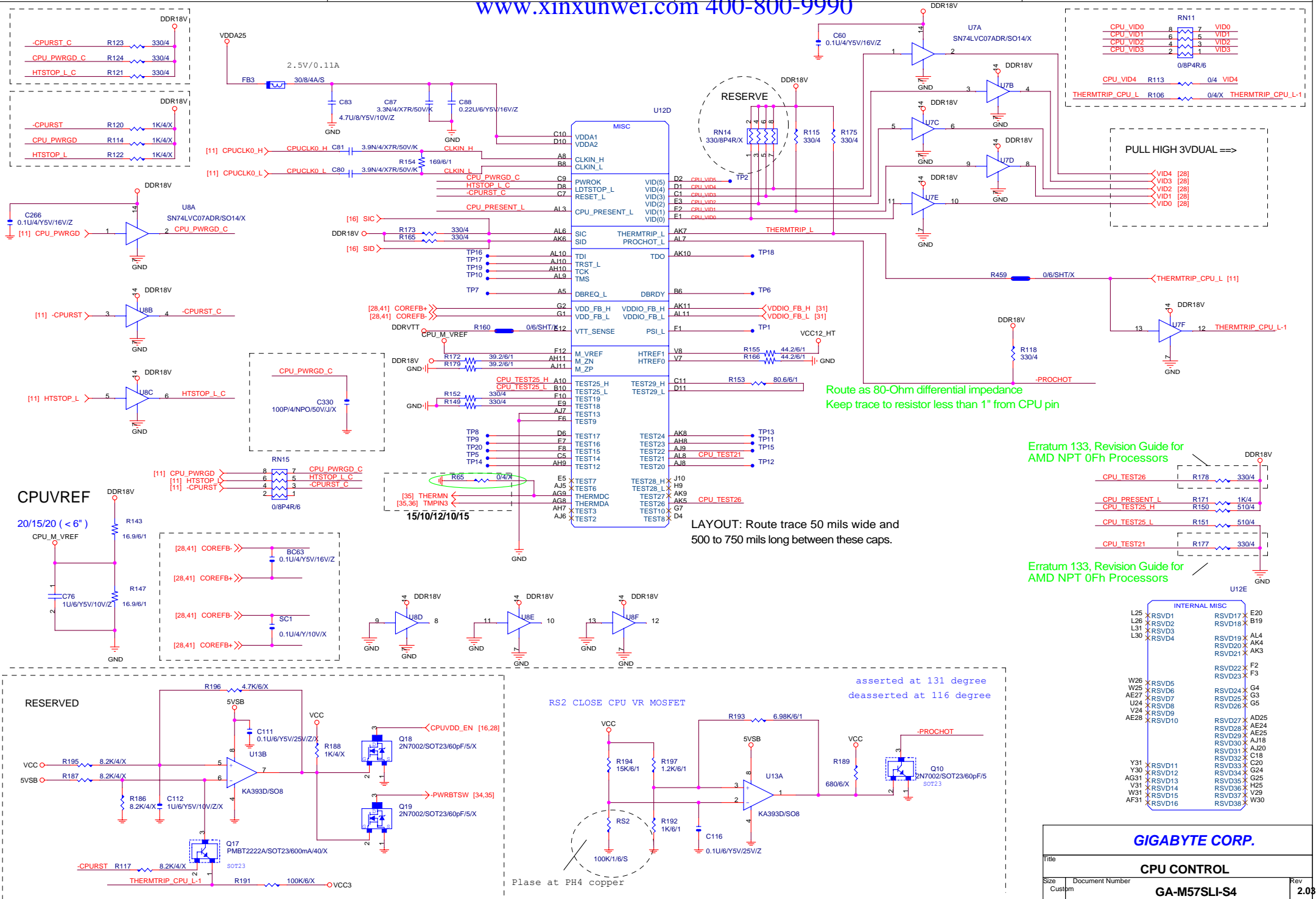
CPU_VDD_RUN = VCORE

VLDT_RUN = VCC12_HT

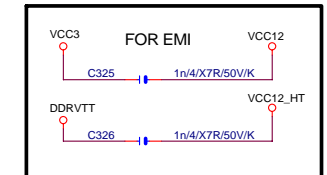
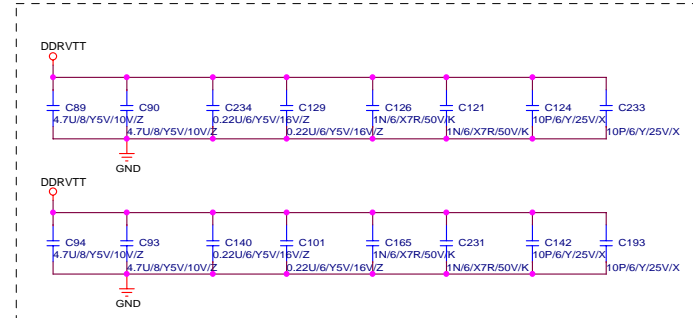
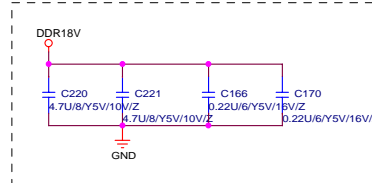
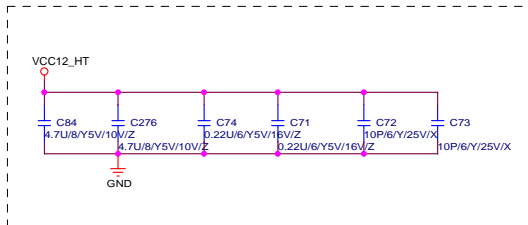
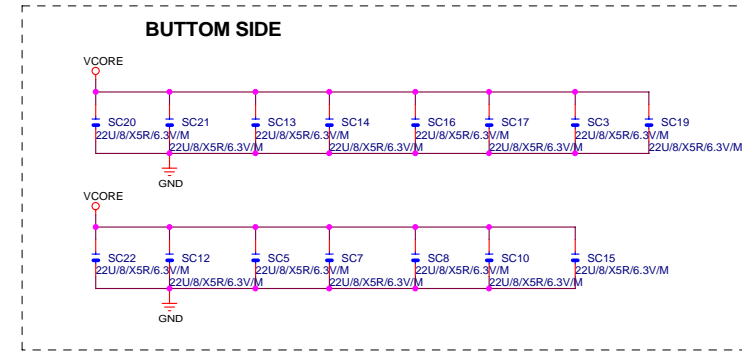
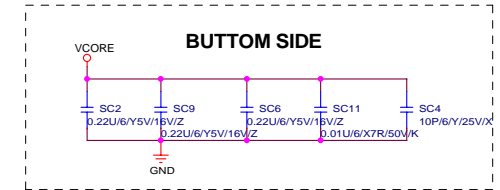
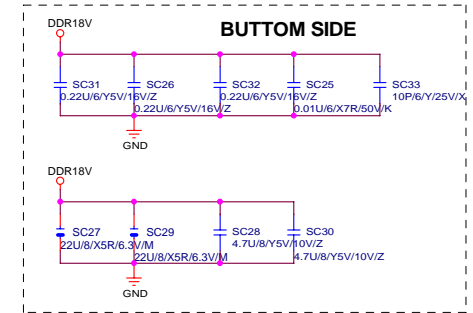
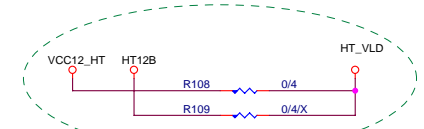
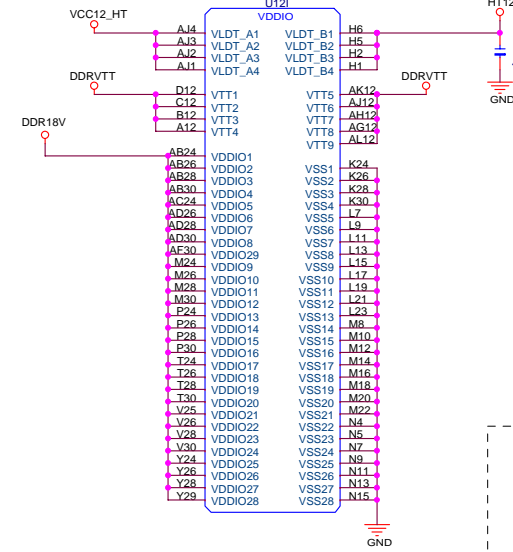
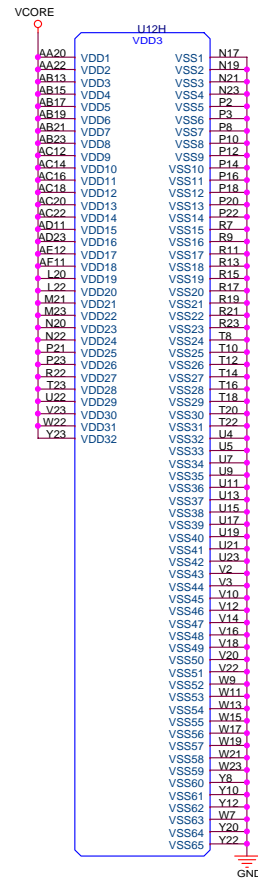
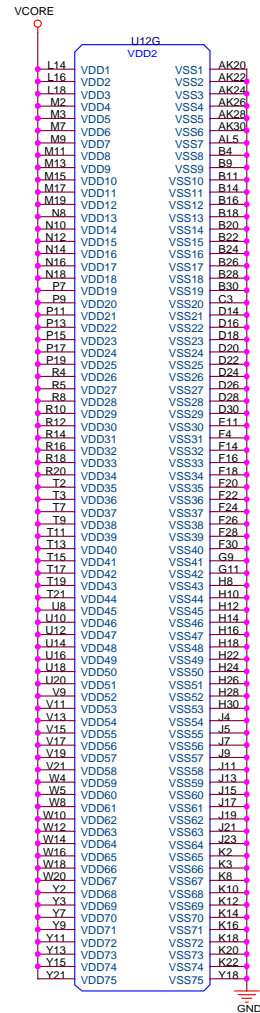
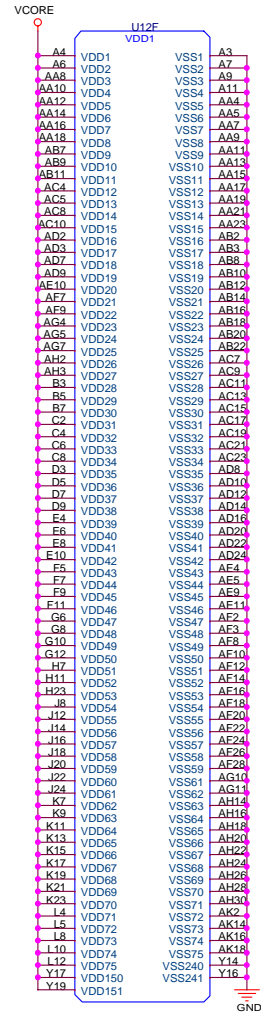
```
VLDT_A = VCC12_HT
VLDT_B = HT12B
```



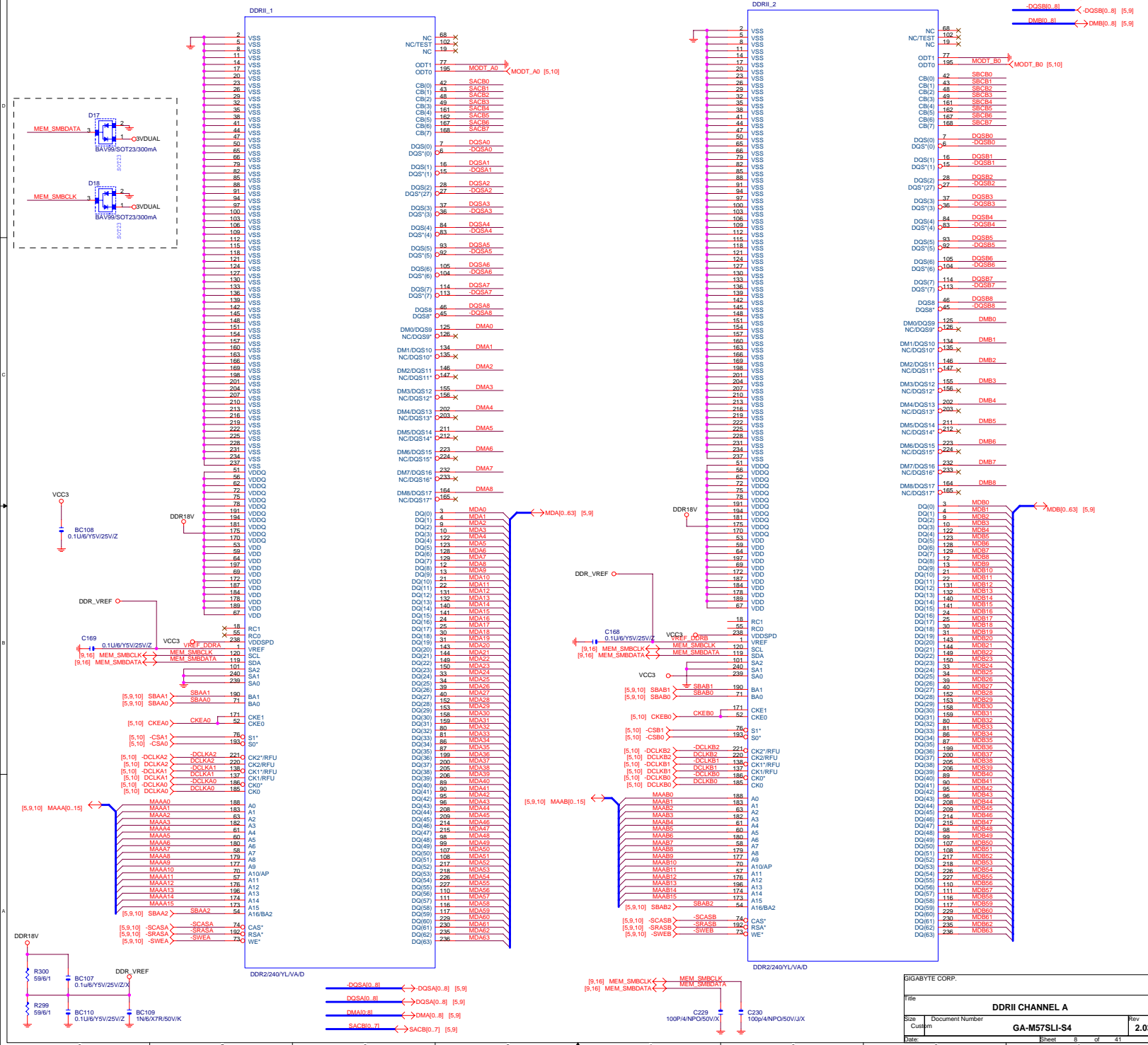


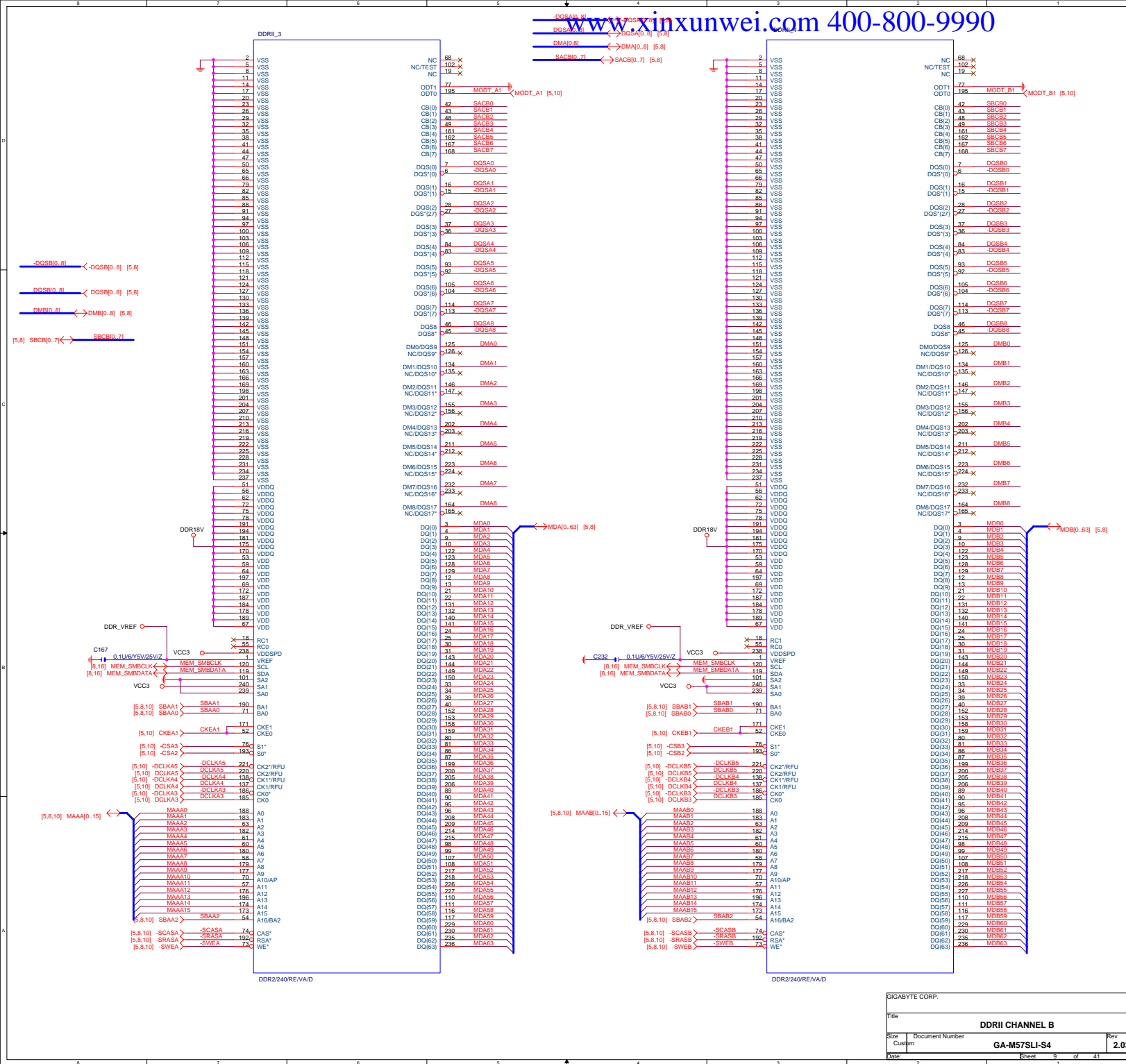


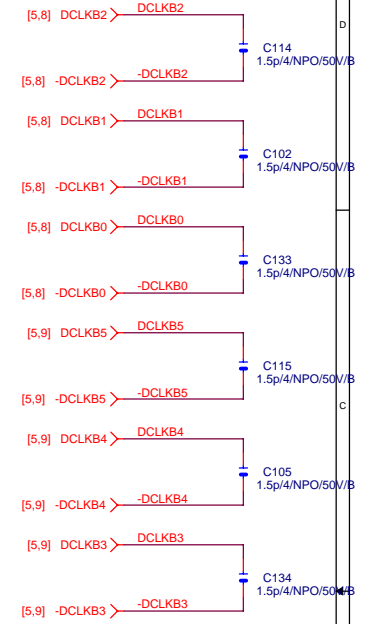
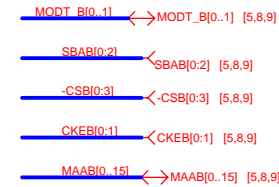
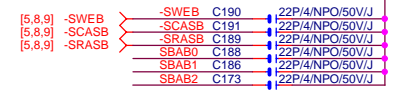
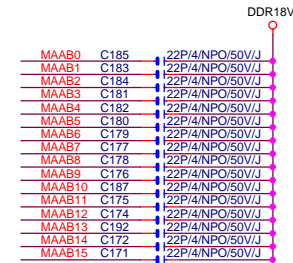
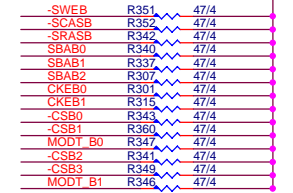
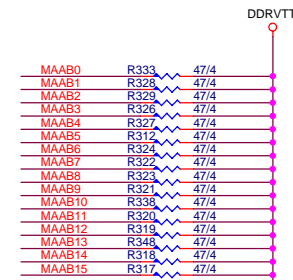
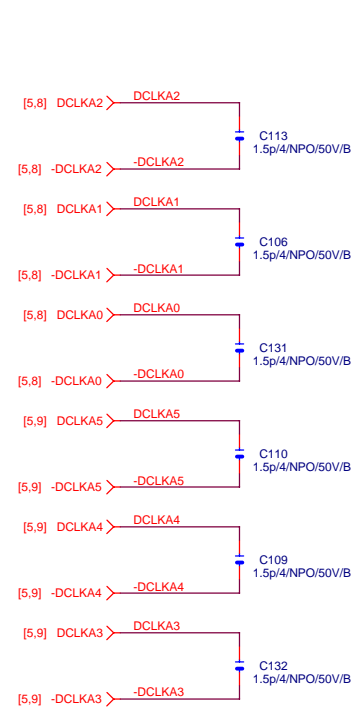
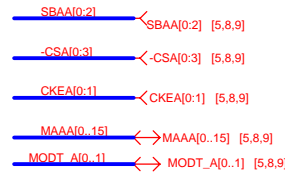
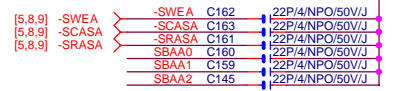
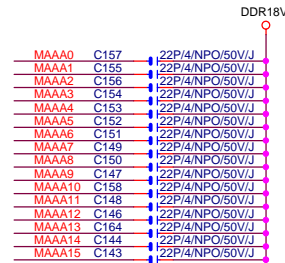
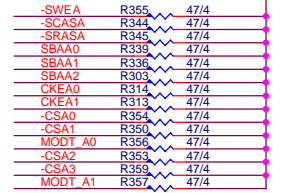
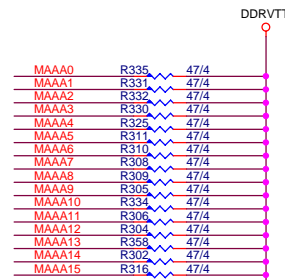
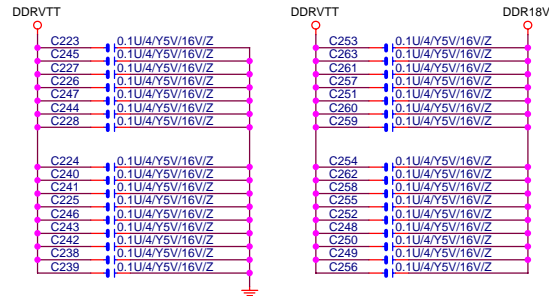
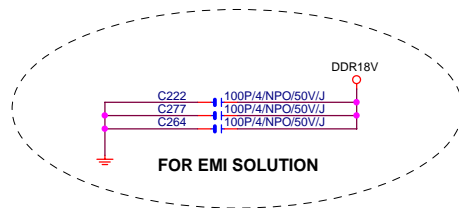
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



GIGABYTE CORP.			
CPU POWER & GND			
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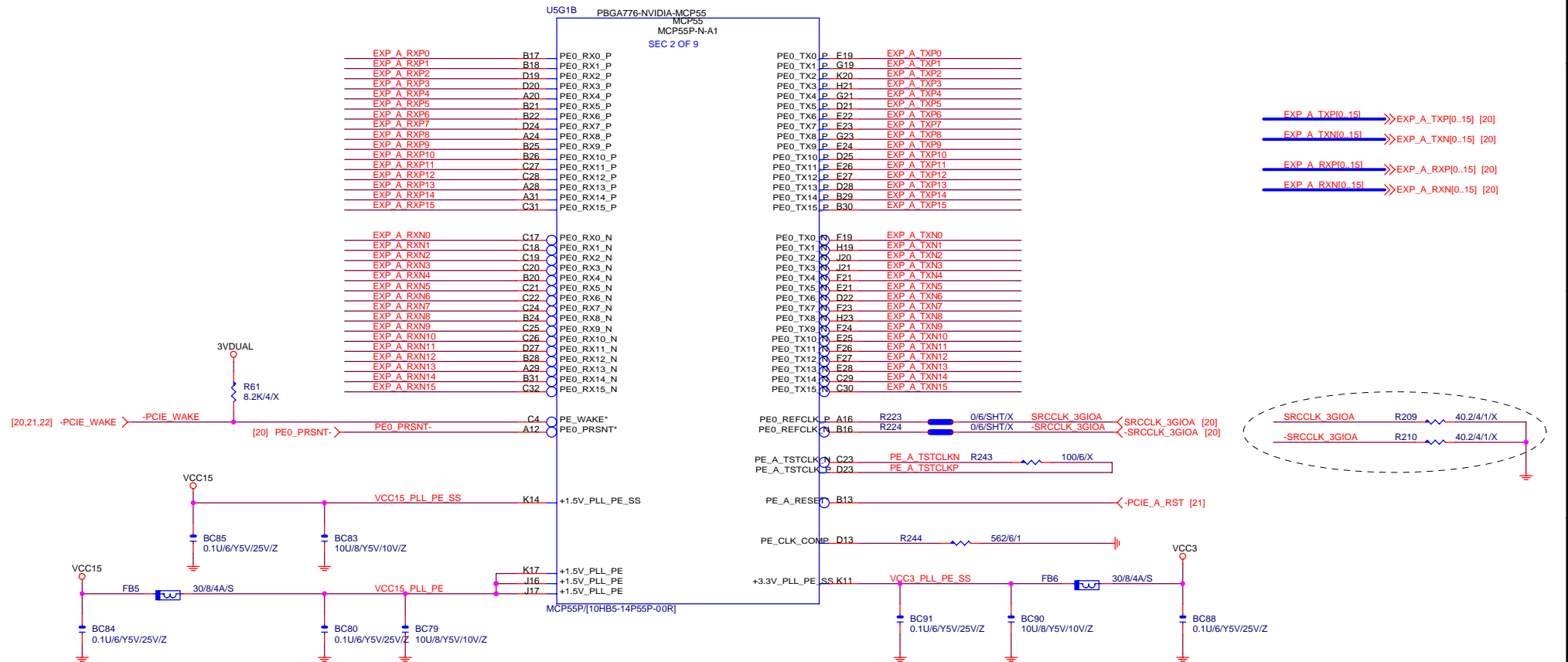




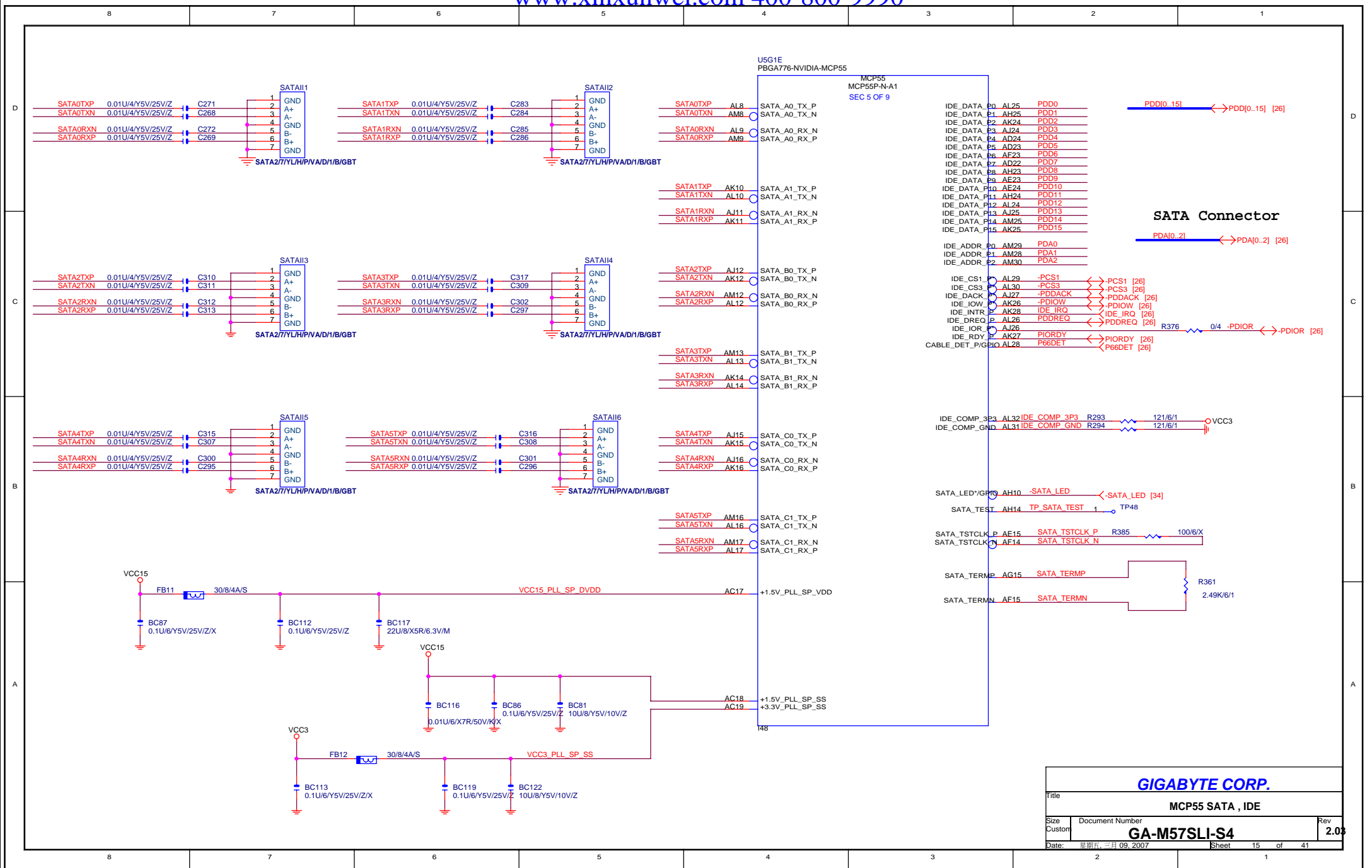


MCP55 HT/CLK

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**GIGABYTE CORP.****MCP55 PCIe X16**

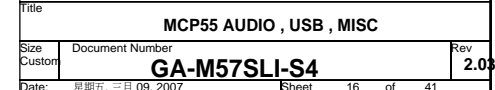
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Size	Document Number			Rev
Custom	GA-M57SLI-S4			2.03
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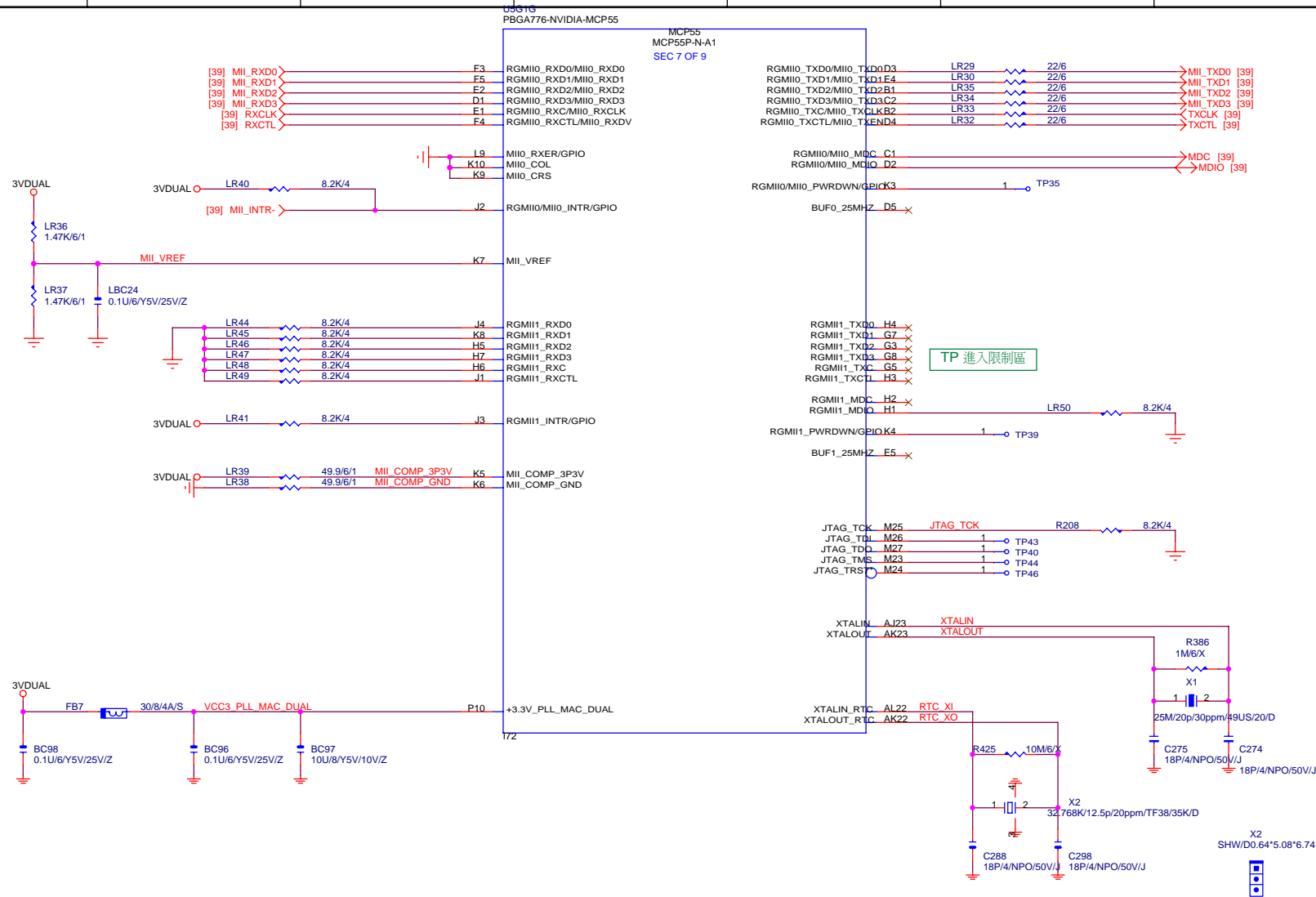


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MCP55 SATA, IDE

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GIGABYTE CORP.

Title

MCP55 DUAL RGMII

Size

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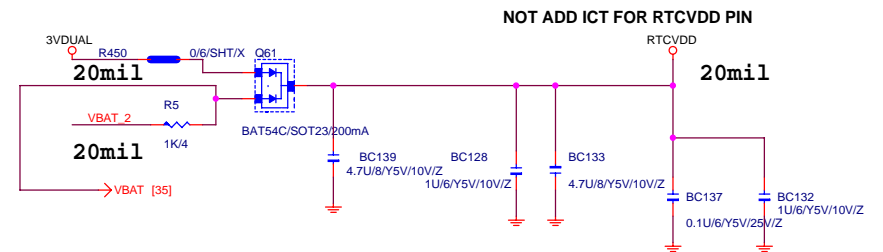
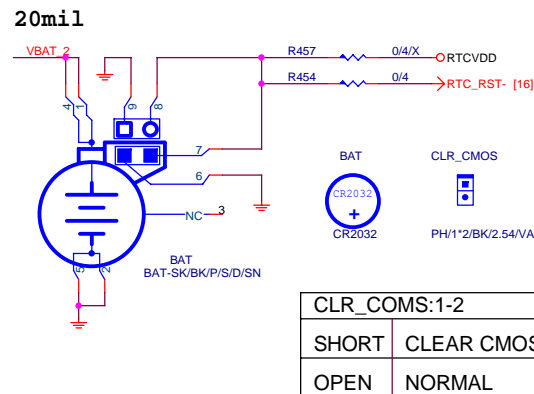
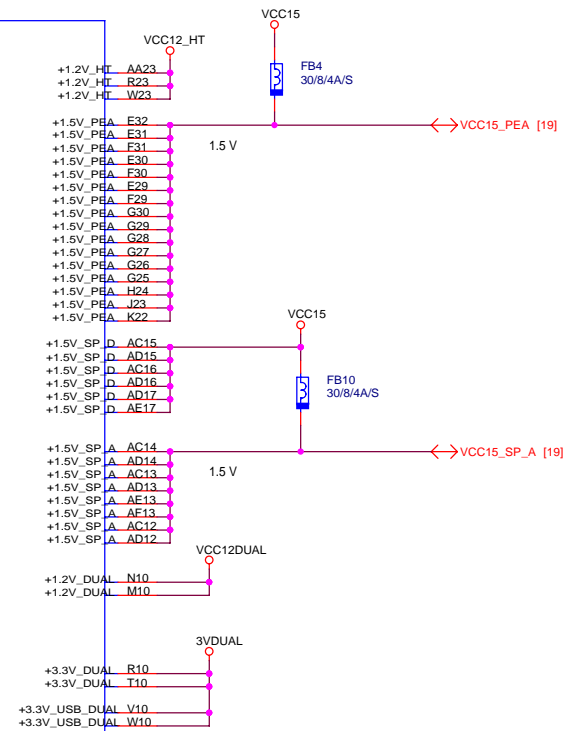
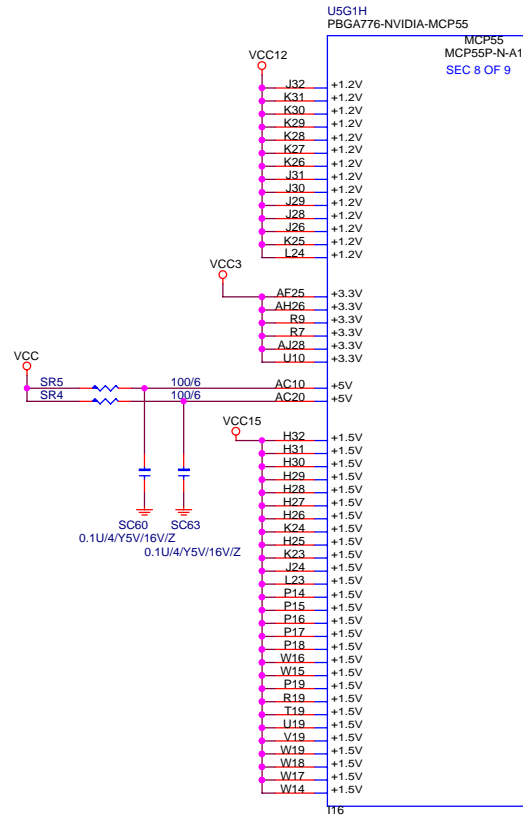
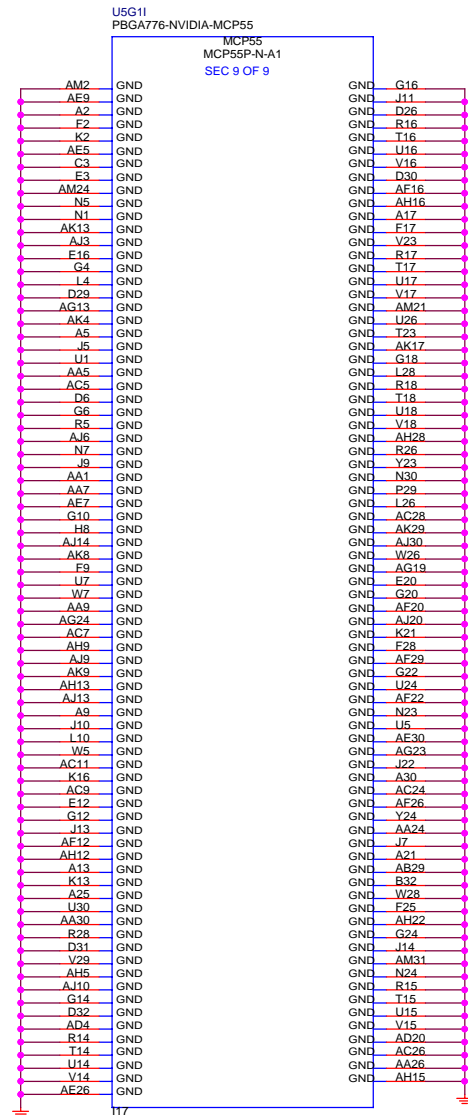
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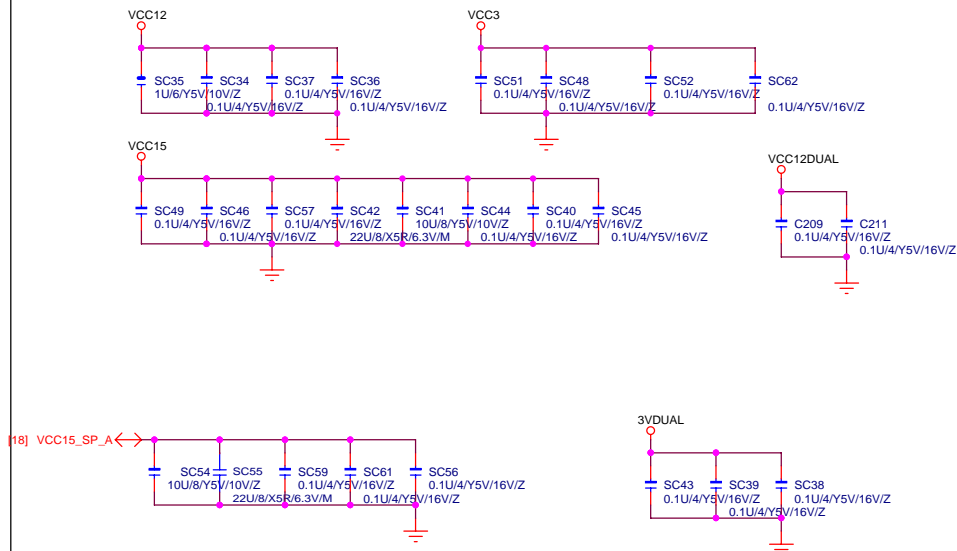


GIGABYTE CORP.

MCP55 PWR/GND

Title				
MCP55 PWR/GND				
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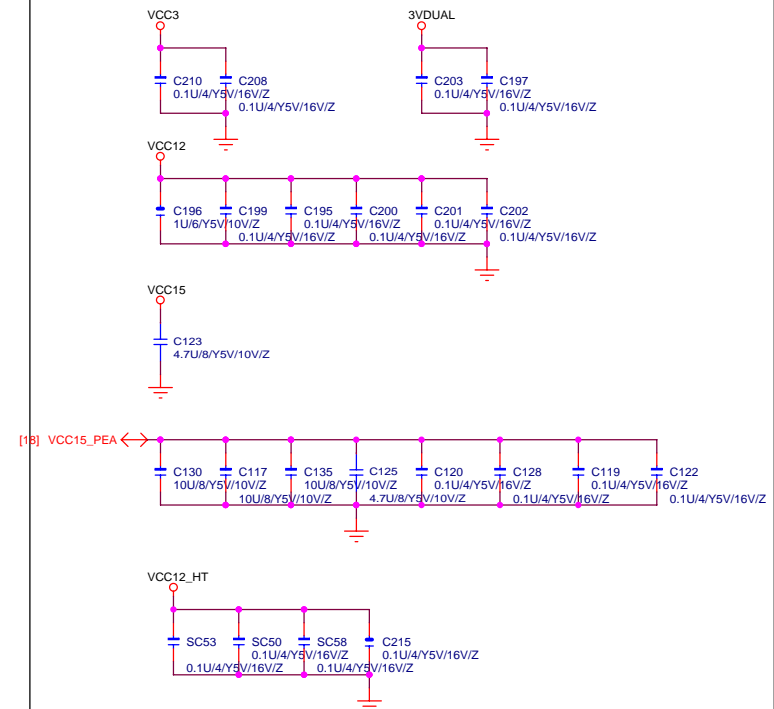
MCP55 BACK SIDE DECOUPLING



MCP55 INTERNAL PULL-UP/PULL-DOWN

PIN	VOLTAGE
A20GATE/GPIO	+3.3V
EXT_SMI*/GPIO	+3.3V_DUAL
HDA_SDATA_IN0/GPIO_22/MGPIO_0	+3.3V_DUAL/GND
HDA_SDATA_IN1/GPIO_23/MGPIO_1	+3.3V_DUAL/GND
HDA_SDATA_IN2/GPIO_24/MGPIO_2	+3.3V_DUAL/GND
HDA_SDATA_OUT/GPIO_45	+3.3V_DUAL/GND
JTAG_TDI	+3.3V
JTAG_TMS	+3.3V
JTAG_TRST*	GND
KBRDRSTIN*/GPIO	+3.3V
PE_WAKE*	+3.3V_DUAL
SIO_PME*/GPIO	+3.3V_DUAL
THERM*/GPIO	+3.3V

MCP55 TOP SIDE DECOUPLING

**GIGABYTE CORP.**

Title

MCP55 DECOUPLING

Size
Custom

Document Number

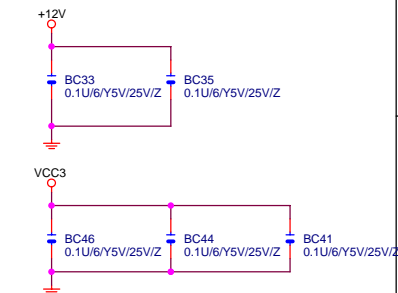
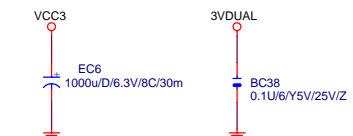
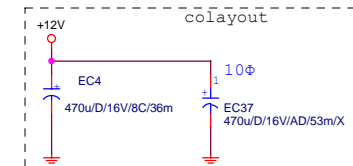
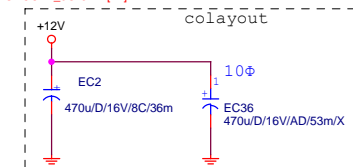
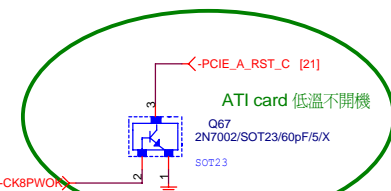
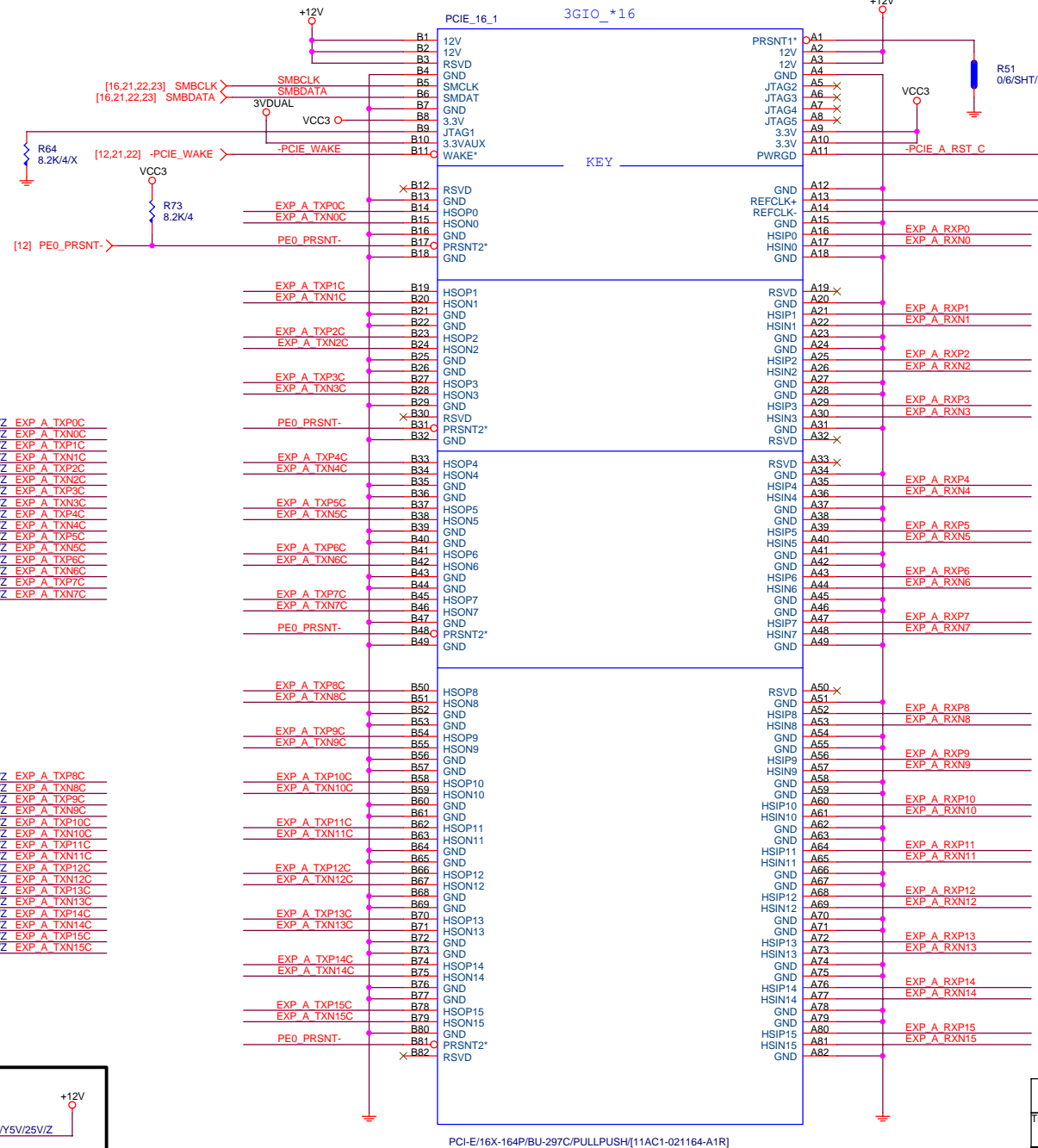
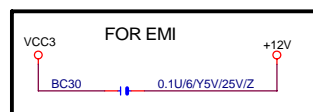
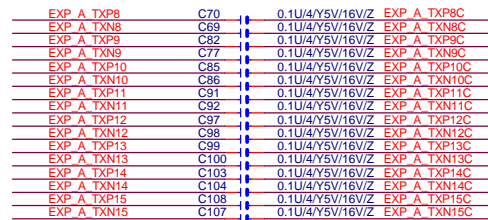
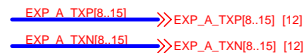
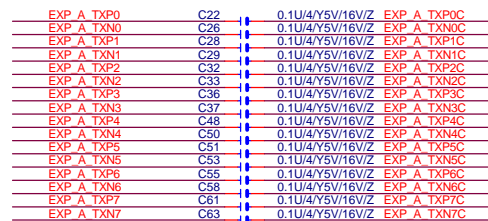
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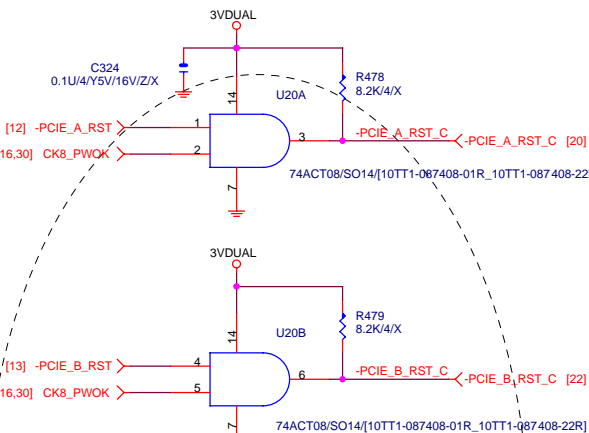
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EXP_B_TXP0	C17	0.1U/4/Y5V/16V/Z	EXP_B_TXP0C
EXP_B_TXN0	C21	0.1U/4/Y5V/16V/Z	EXP_B_TXN0C
EXP_B_TXP1	C30	0.1U/4/Y5V/16V/Z	EXP_B_TXP1C
EXP_B_TXN1	C31	0.1U/4/Y5V/16V/Z	EXP_B_TXN1C
EXP_B_TXP2	C34	0.1U/4/Y5V/16V/Z	EXP_B_TXP2C
EXP_B_TXN2	C35	0.1U/4/Y5V/16V/Z	EXP_B_TXN2C
EXP_B_TXP3	C38	0.1U/4/Y5V/16V/Z	EXP_B_TXP3C
EXP_B_TXN3	C39	0.1U/4/Y5V/16V/Z	EXP_B_TXN3C
EXP_B_TXP4	C46	0.1U/4/Y5V/16V/Z	EXP_B_TXP4C
EXP_B_TXN4	C49	0.1U/4/Y5V/16V/Z	EXP_B_TXN4C
EXP_B_TXP5	C52	0.1U/4/Y5V/16V/Z	EXP_B_TXP5C
EXP_B_TXN5	C54	0.1U/4/Y5V/16V/Z	EXP_B_TXN5C
EXP_B_TXP6	C56	0.1U/4/Y5V/16V/Z	EXP_B_TXP6C
EXP_B_TXN6	C59	0.1U/4/Y5V/16V/Z	EXP_B_TXN6C
EXP_B_TXP7	C62	0.1U/4/Y5V/16V/Z	EXP_B_TXP7C
EXP_B_TXN7	C64	0.1U/4/Y5V/16V/Z	EXP_B_TXN7C

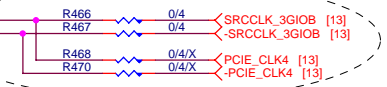
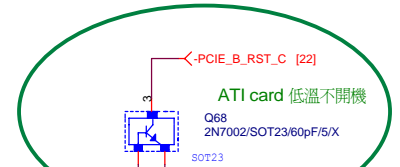
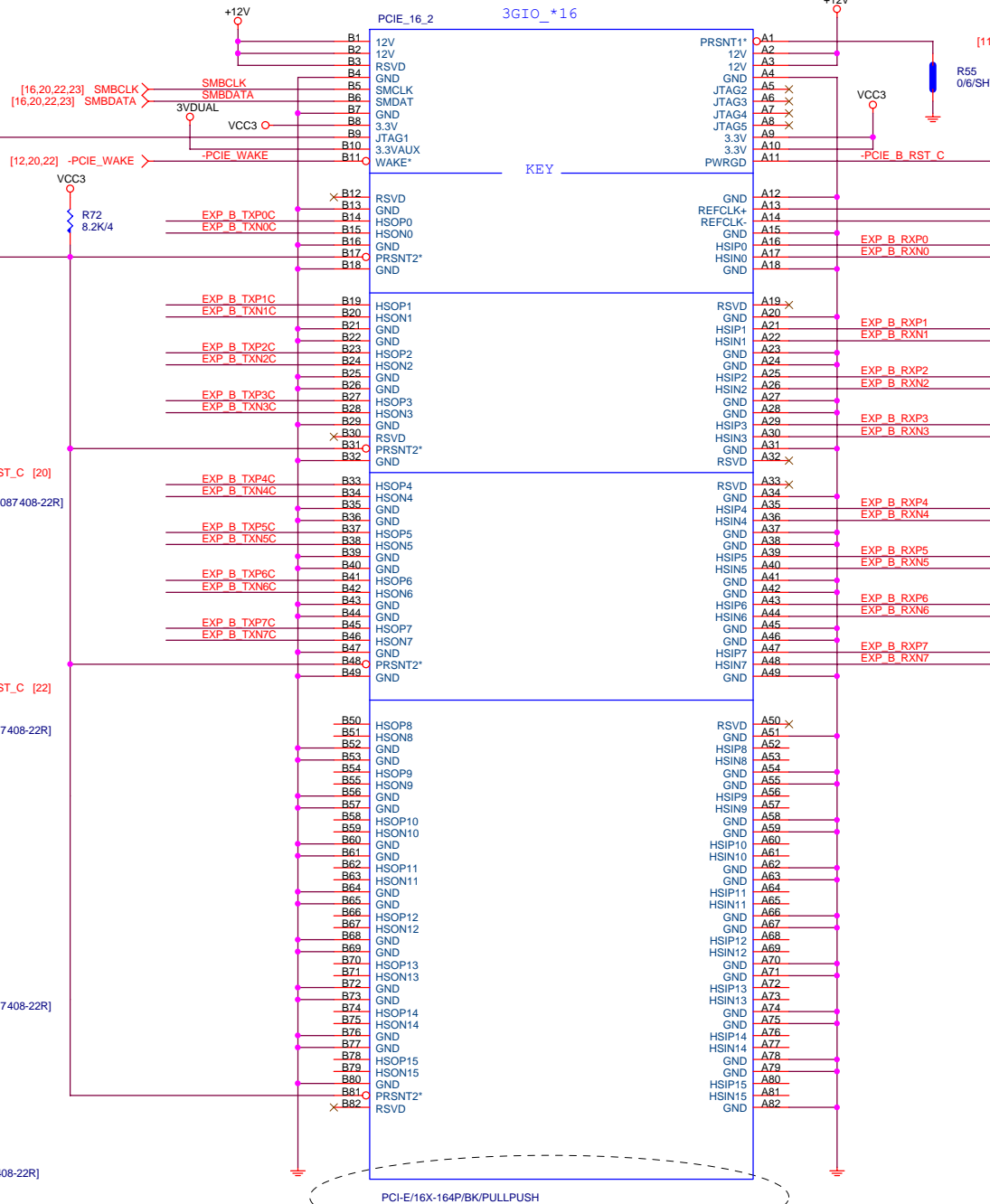
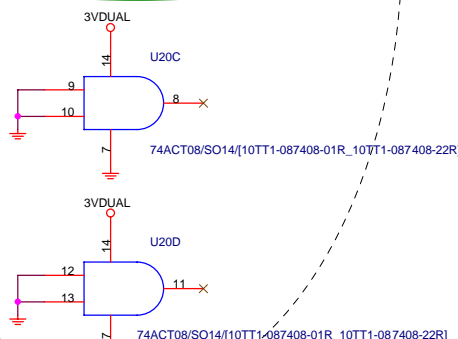
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EXP_B_TXN0_71 >> EXP_B_TXN[0..7] [13]

[13] PE5_PRSNT- R469 0/4
[13] PE4_PRSNT- R471 0/4/X

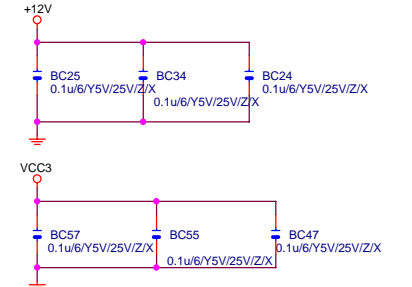
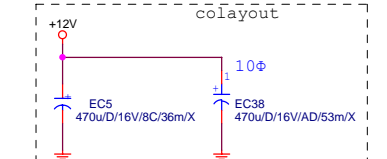
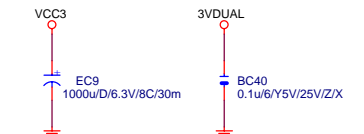
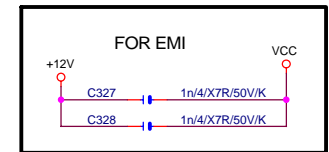


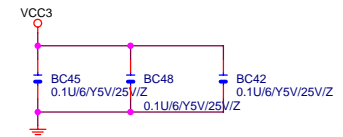
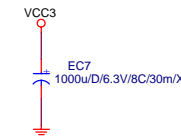
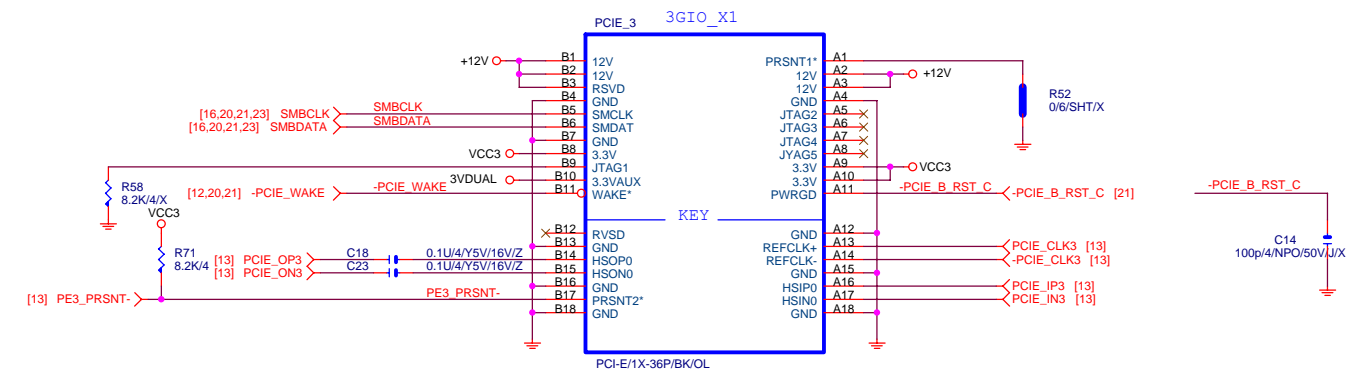
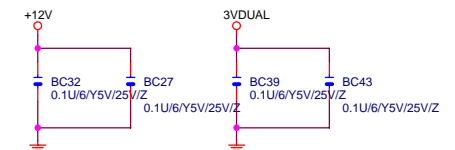
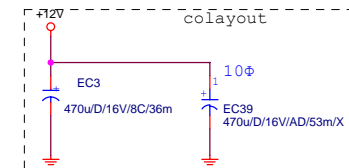
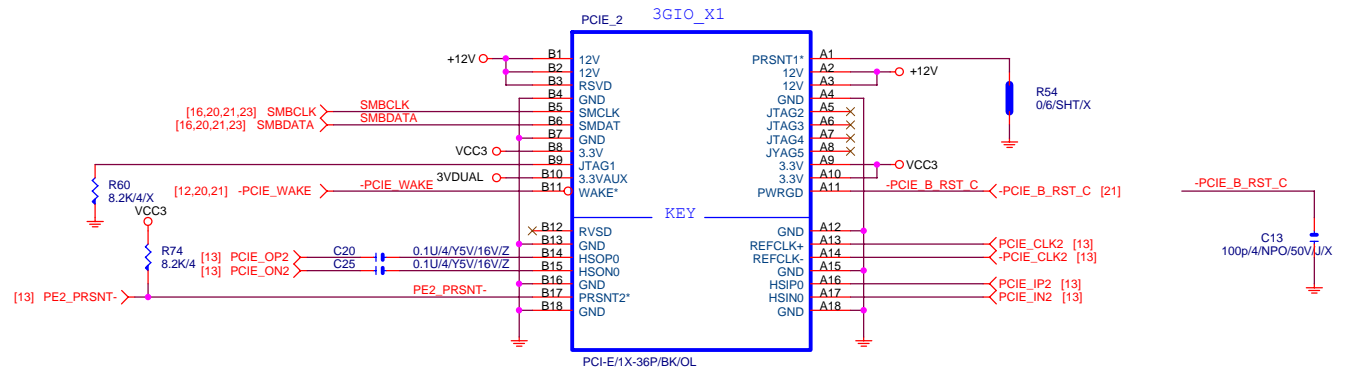
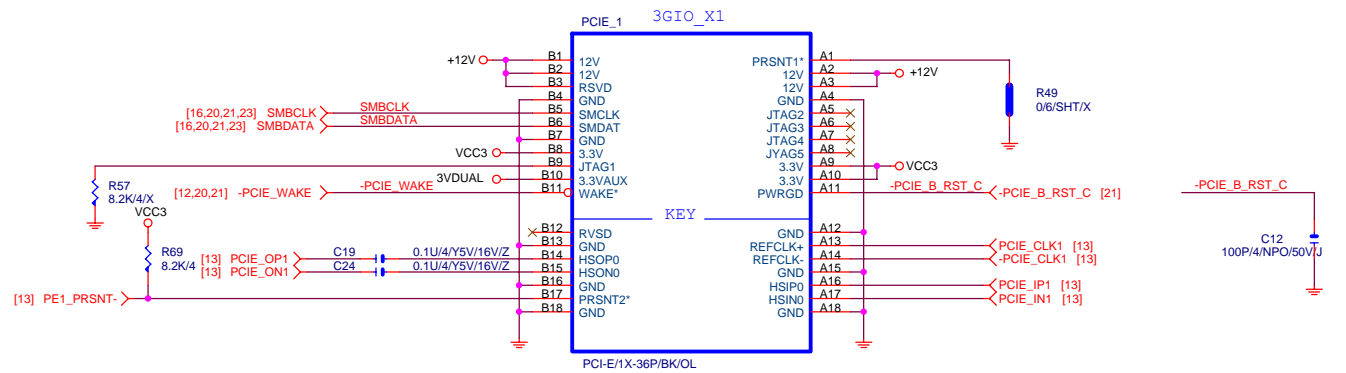
PCIE_A_RST R480 0/4/X PCIE_A_RST_C
PCIE_B_RST R481 0/4/X PCIE_B_RST_C

**VCC3 10% to Core power 90% < 30ms
else, PCIE_RST add 74ACT08**



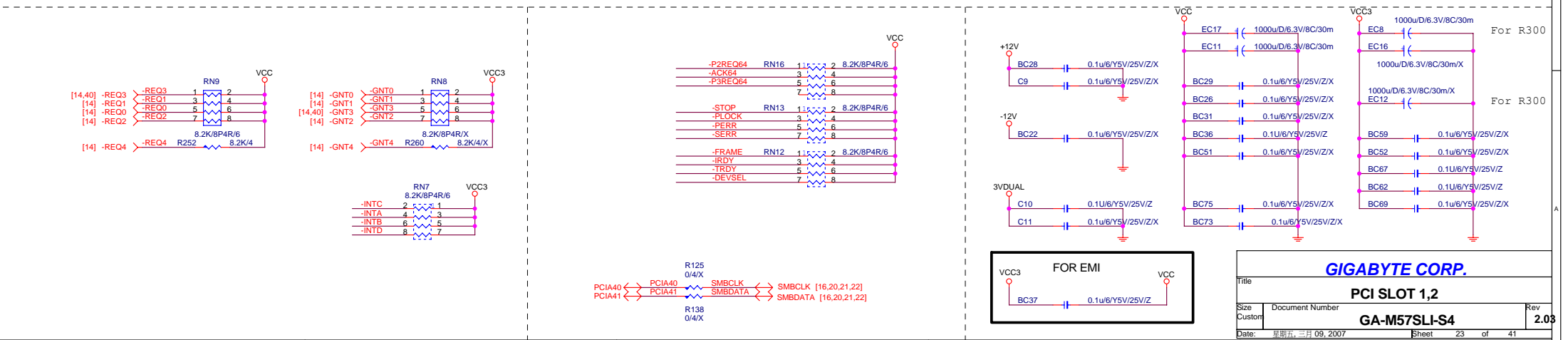
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EXP_B_RXN0_71 >> EXP_B_RXN[0..7] [13]

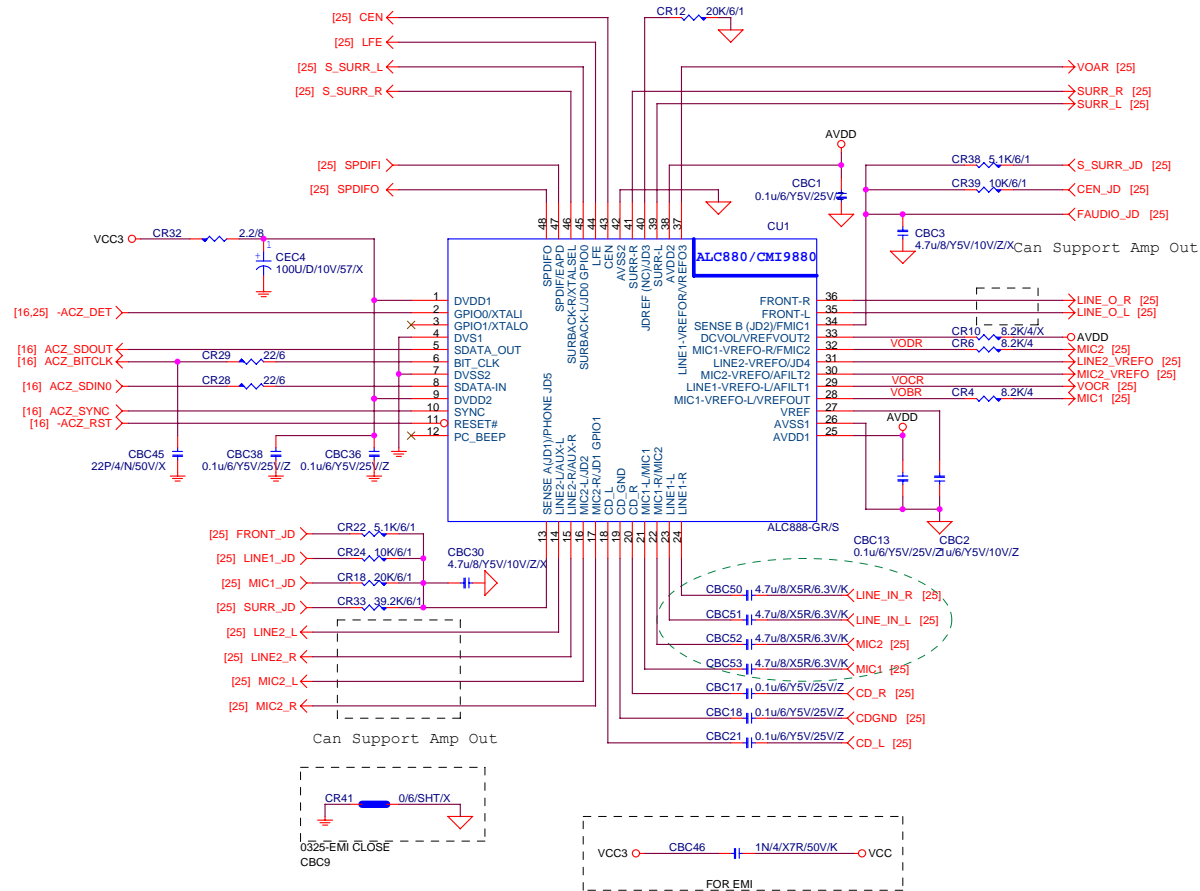




GIGABYTE CORP.

Title		
PCI E SLOT 1, 2		
GA-M57SLI-S4		
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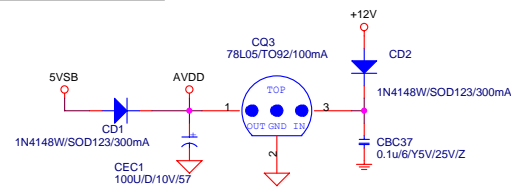




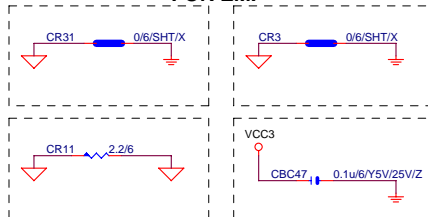
GIGABYTE CORP.

Title			
AZALIA-ALC888			
Size	Document Number	Rev	
Custom	GA-M57SLI-S4	2.03	
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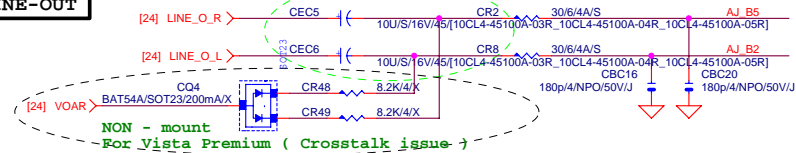
CODEC POWER/EMI PAD



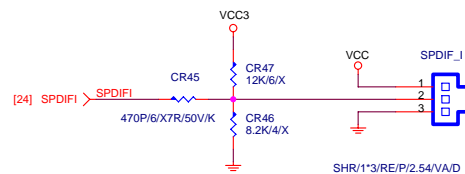
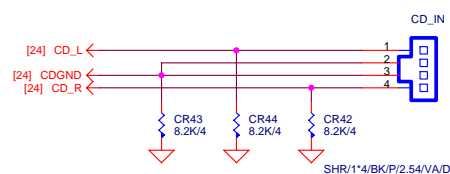
FOR EMI



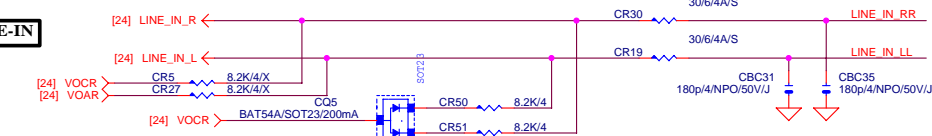
LINE-OUT



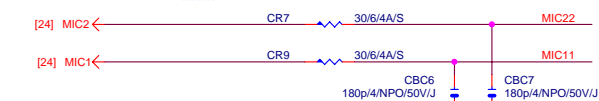
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100	100



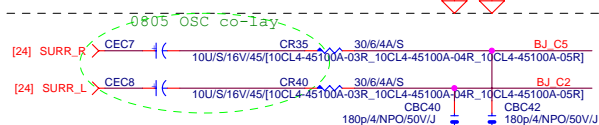
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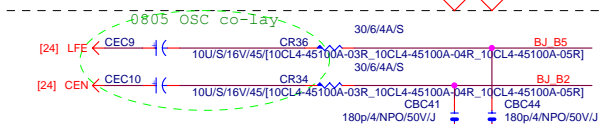
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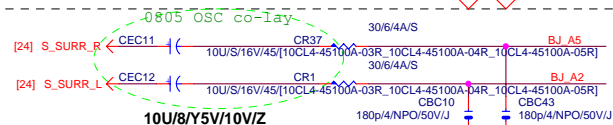
SURROUND



CEN/LFE

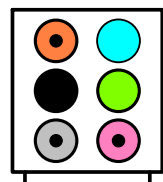


SURR BACK

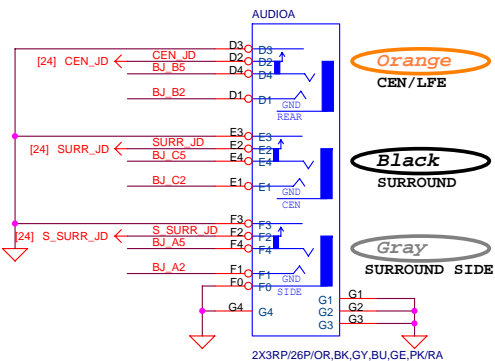
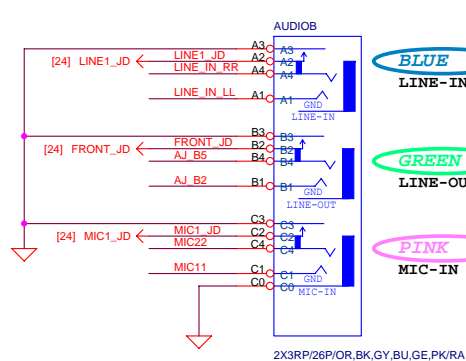
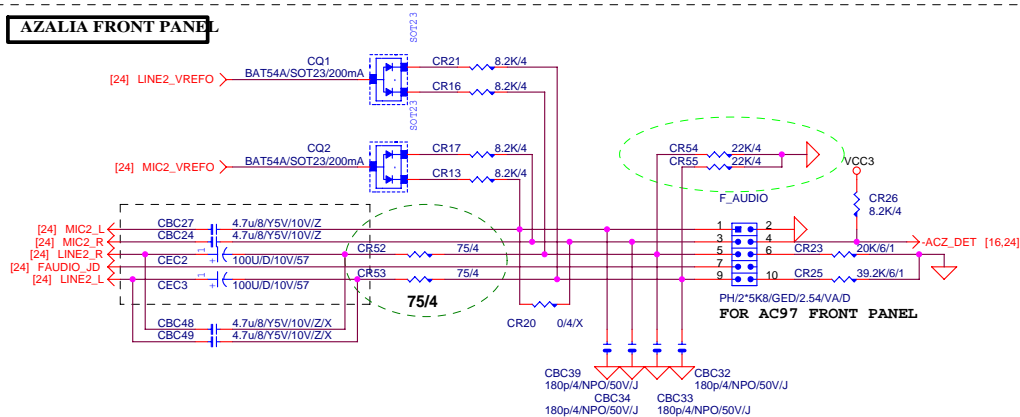


AZALIA JACK

BTX AZALIA CONNECTOR

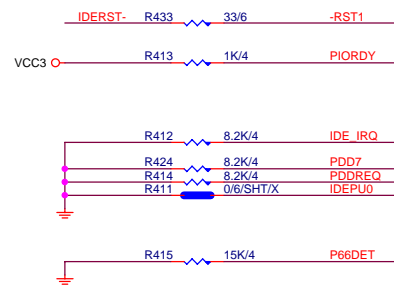
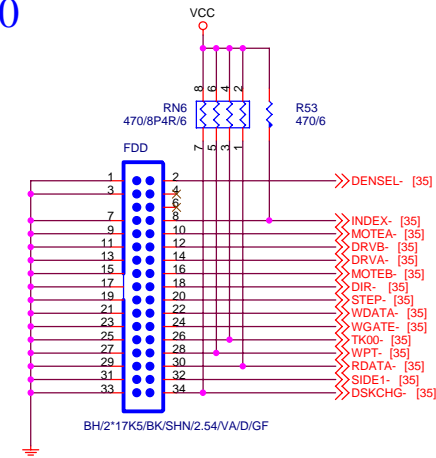
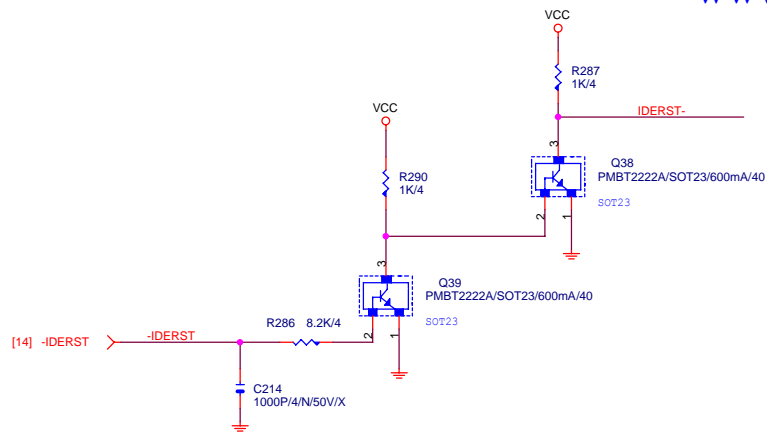


11NR6-403007-21

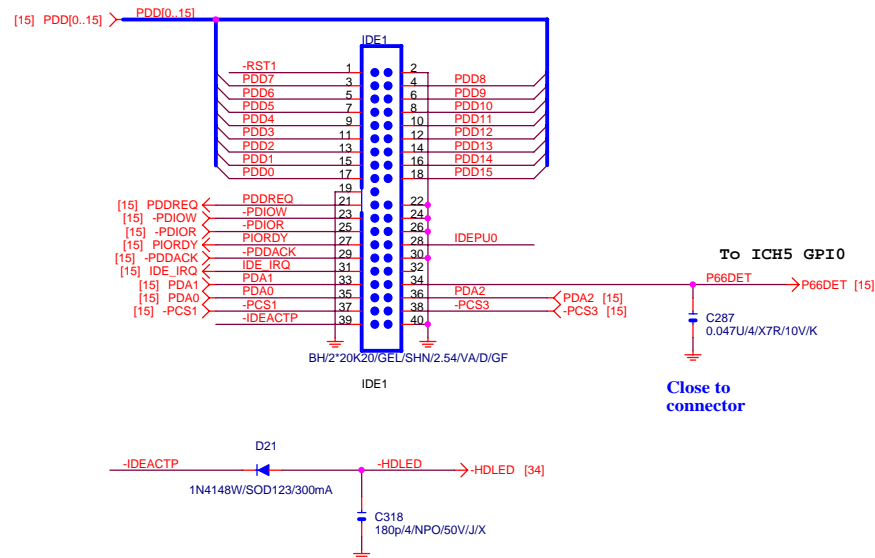
**AZALIA FRONT PANEL**

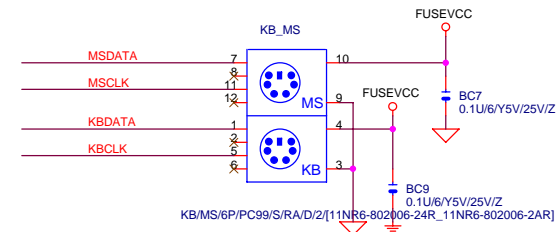
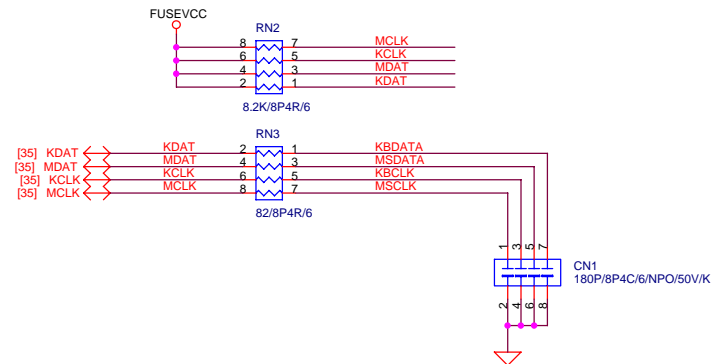
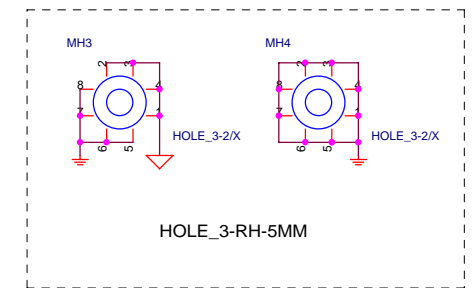
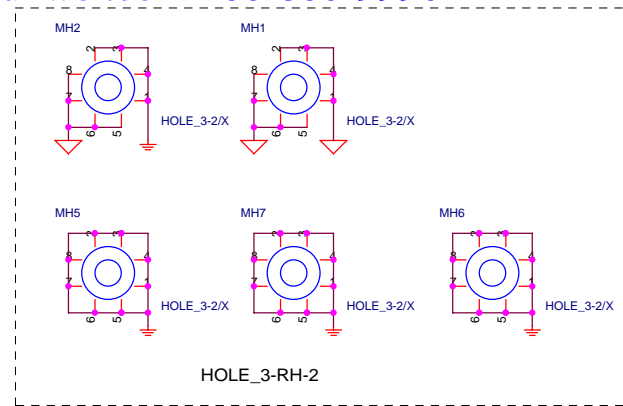
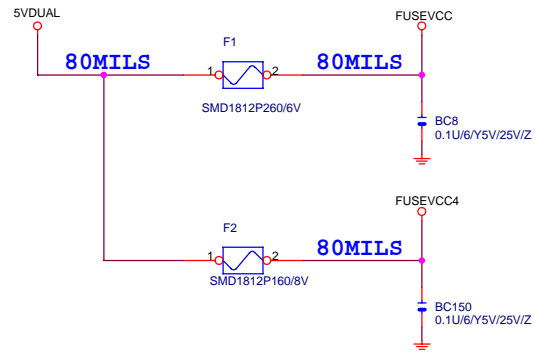
GIGABYTE CORP.

Title			
AUDIO JACK			
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PRIMARY IDE CONNECTOR





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Title

KB & PS2 MOUSE & IR

Size

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2.03

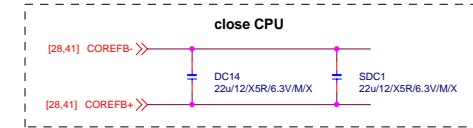
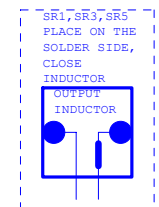
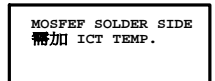
Date:

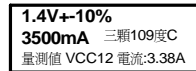
Sheet

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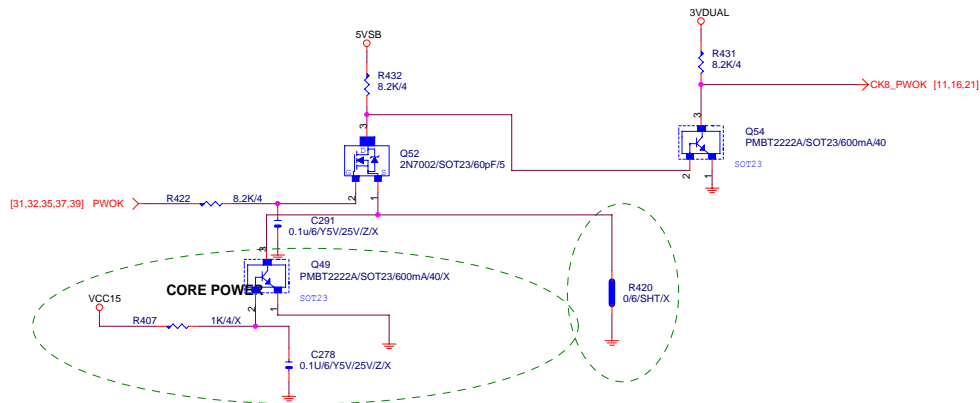
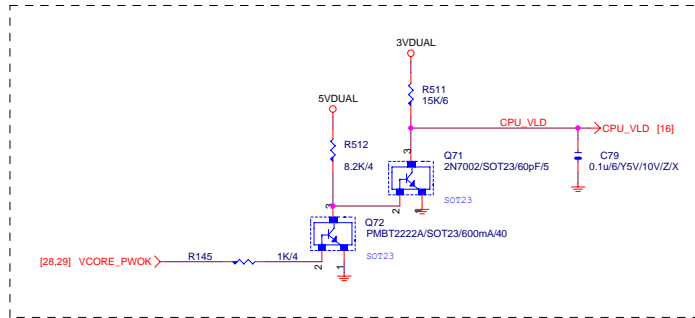
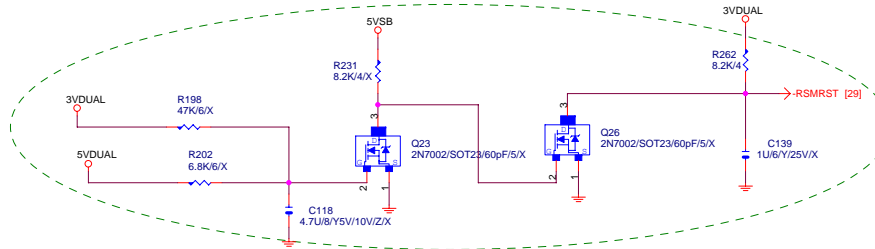
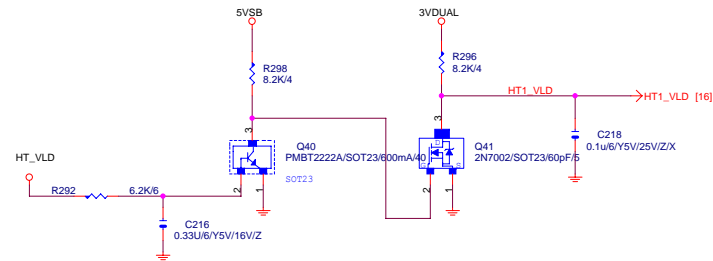
of

41



$$1.25(1+12/100)=1.4V$$


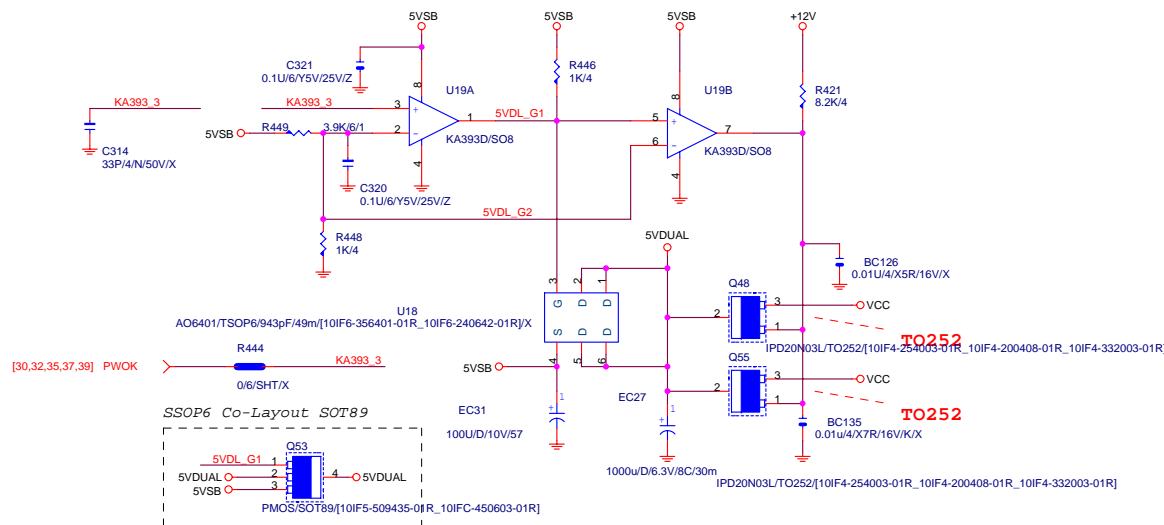
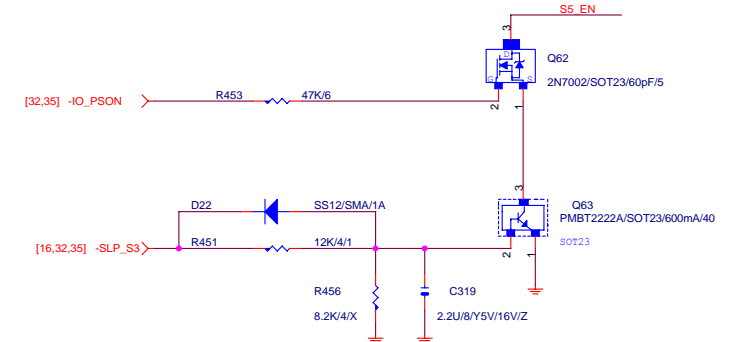
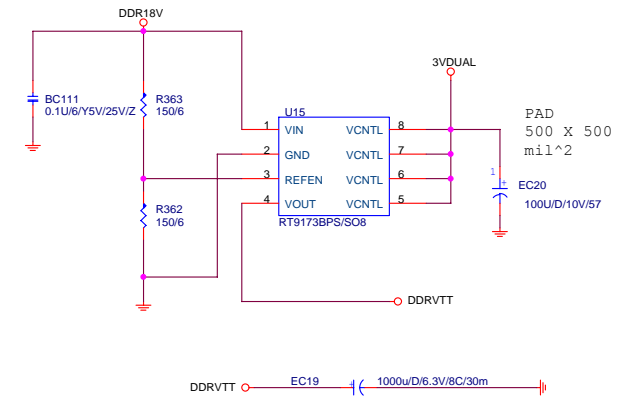
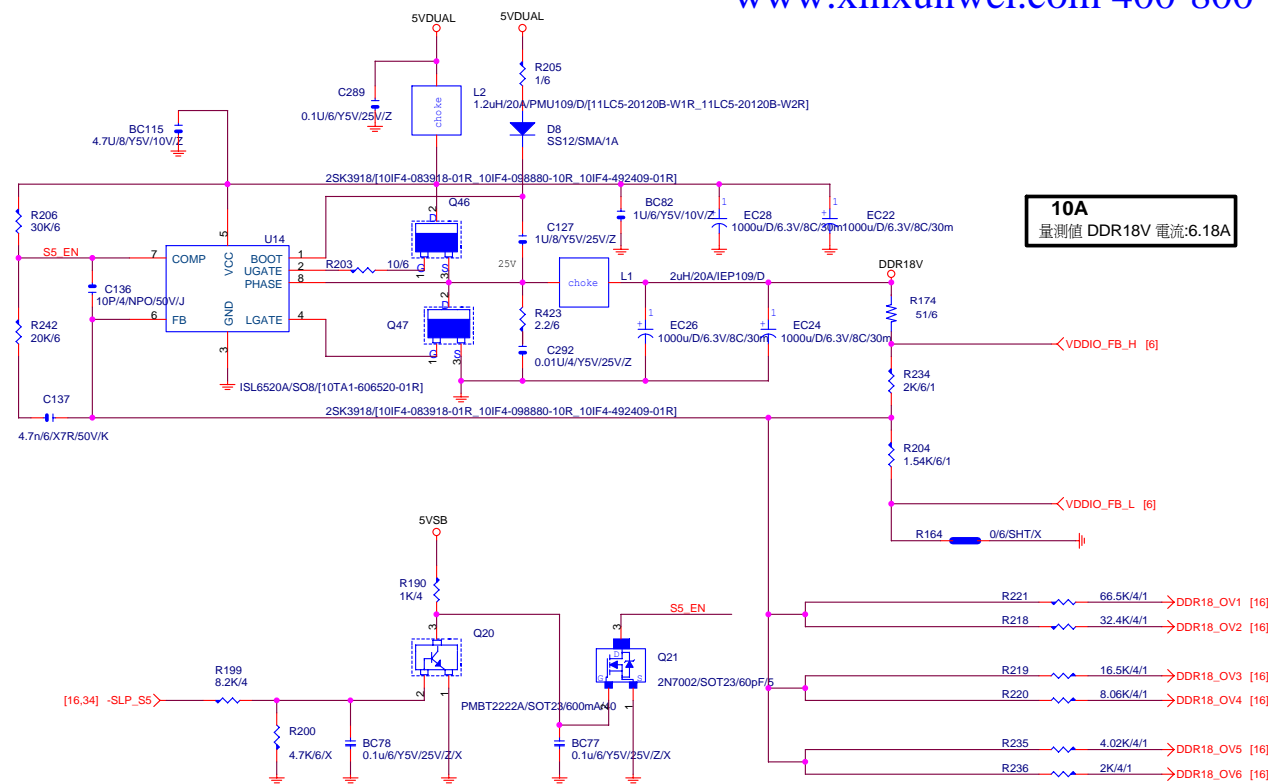
Title			
VCC12 HT,VCCA25,PLL POWER			
Size	Document Number		Rev
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A

B

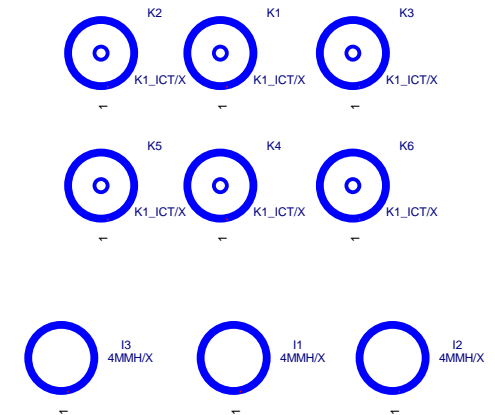
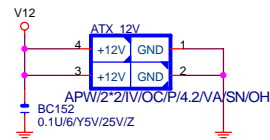
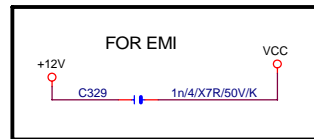
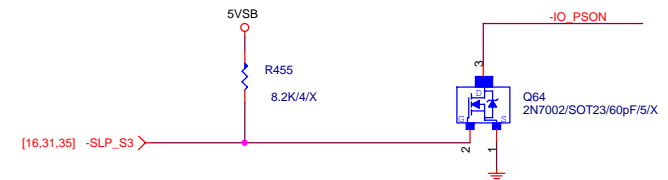
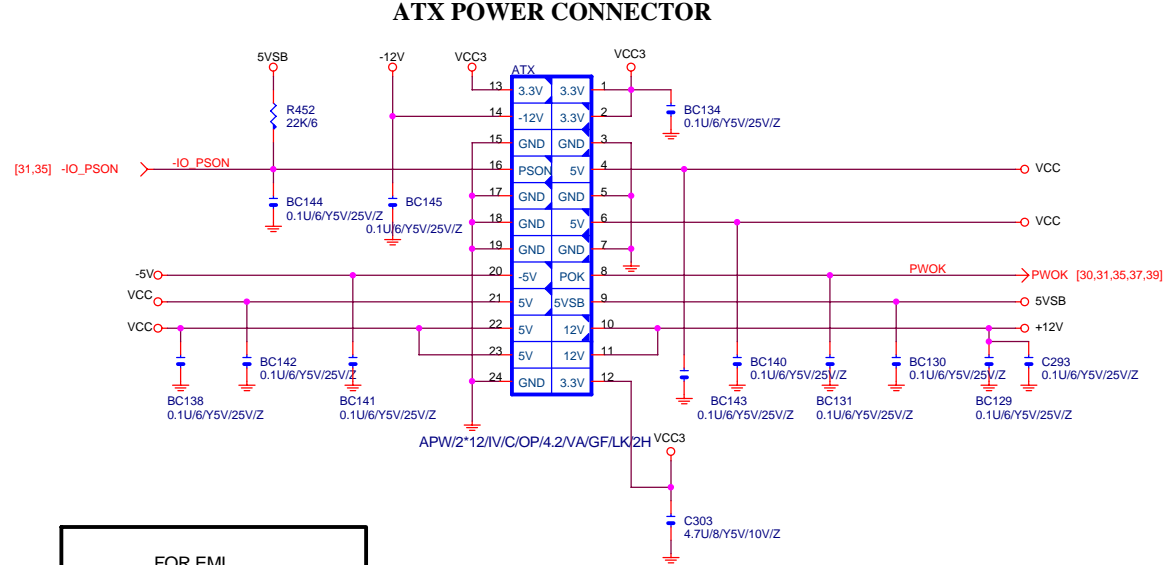
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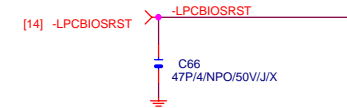
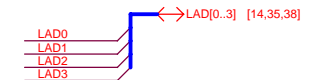
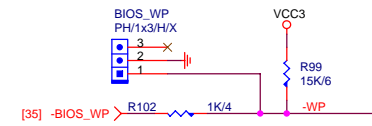
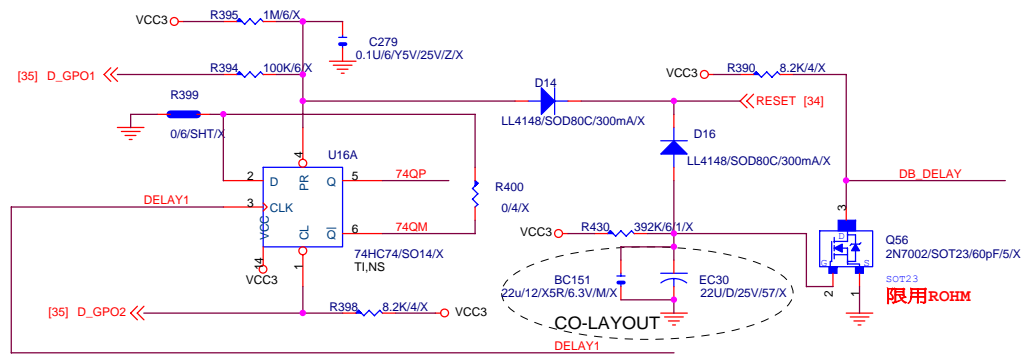


	G2	S5/S4	S3	S1/S0
-SLP_S5	H	L	H	H
-IO_PSON	H	H	H	L
-SLP_S3	H	L	L	H
DDR18V				

GIGABYTE CORP.			
Title DDR18 , DDRVTT , 5VDUAL			
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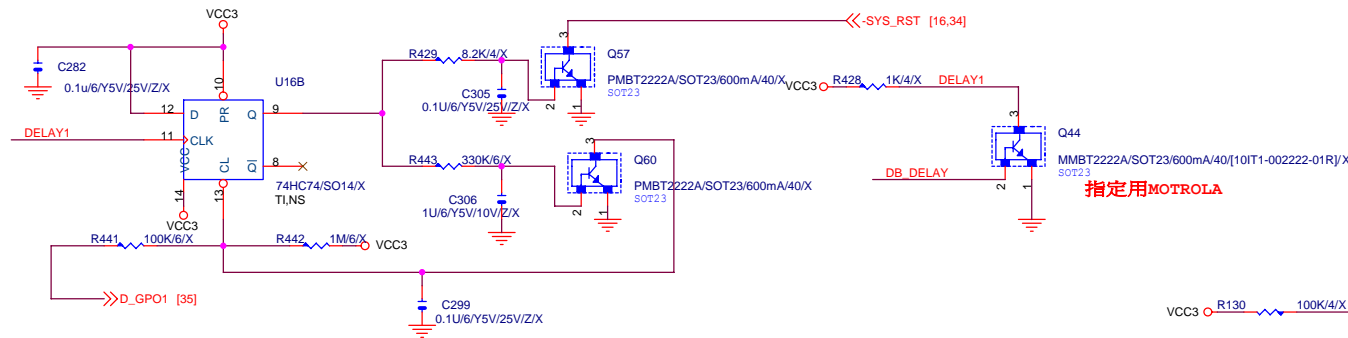
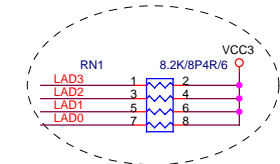
ATX POWER CONNECTOR



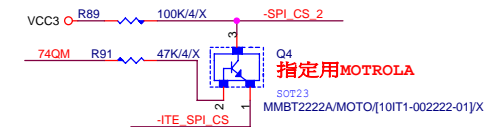


DUAL BIOS SELECTION

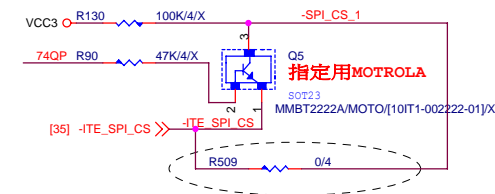
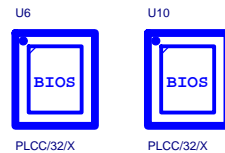
	Main	Backup
GPO30	0	1
GPO28	1	0



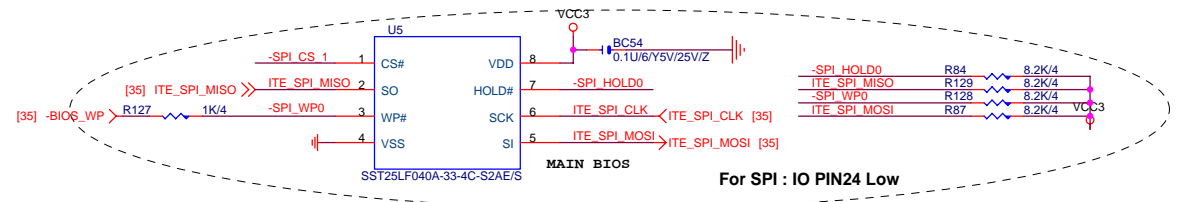
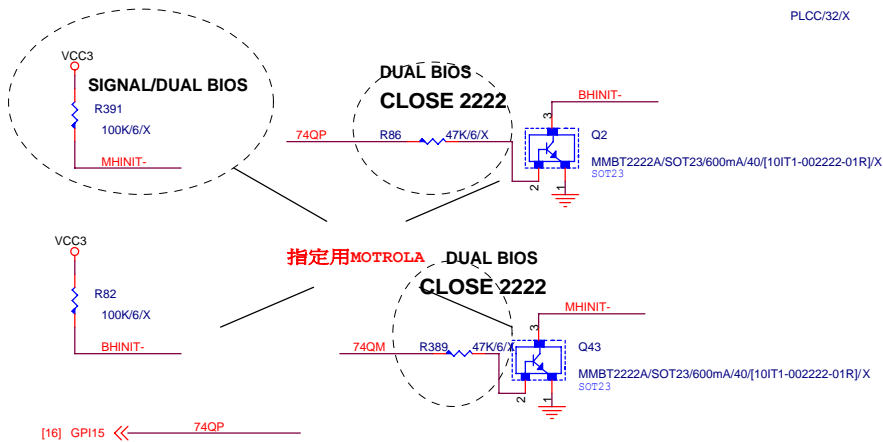
指定用MOTROLA



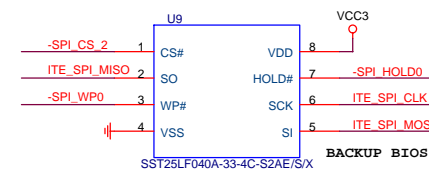
指定用MOTROLA



指定用MOTROLA



For SPI : IO PIN24 Low



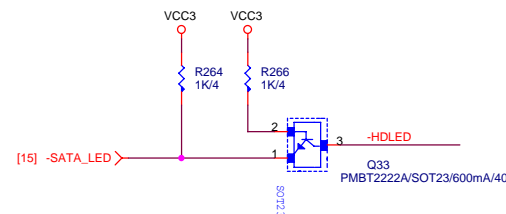
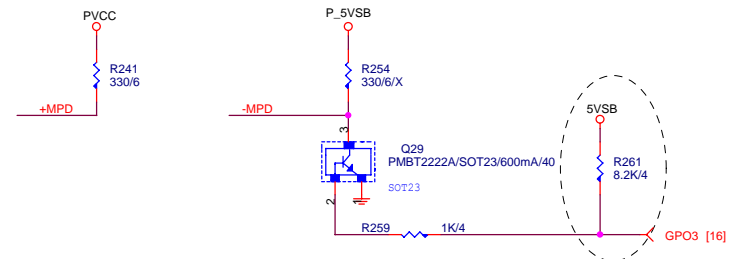
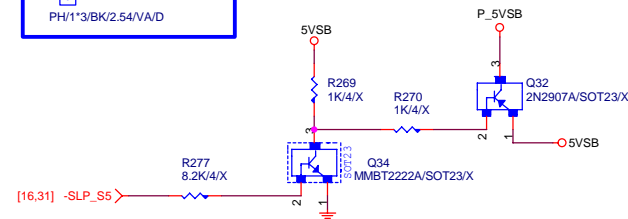
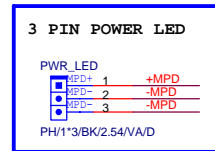
GIGABYTE CORP.

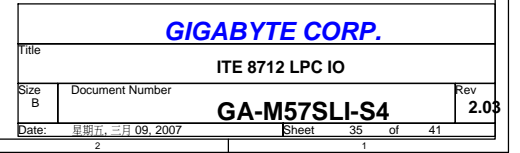
DUAL BIOS

GA-M57SLI-S4

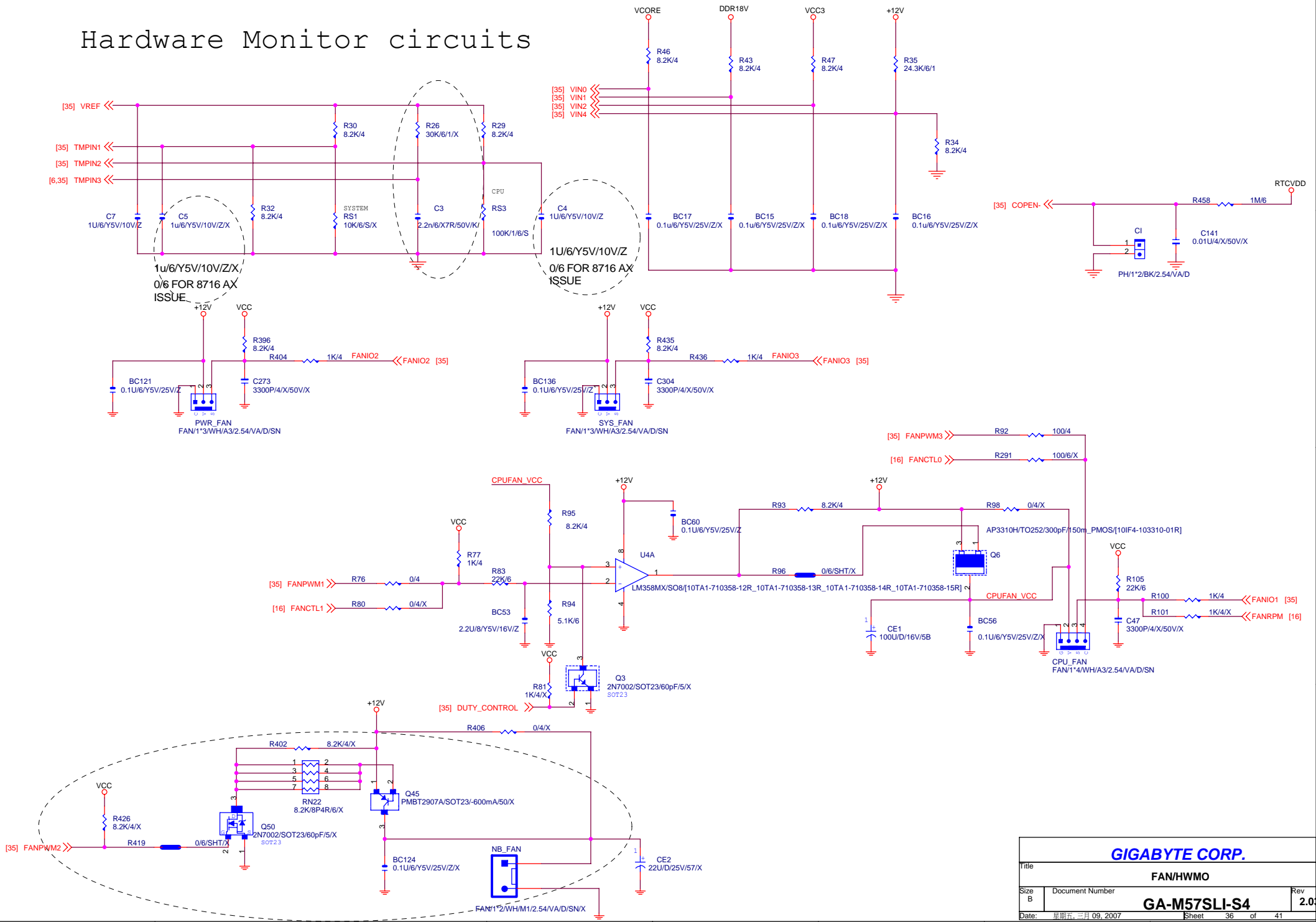
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Hardware Monitor circuits



GIGABYTE CORP.

FAN/HWMO

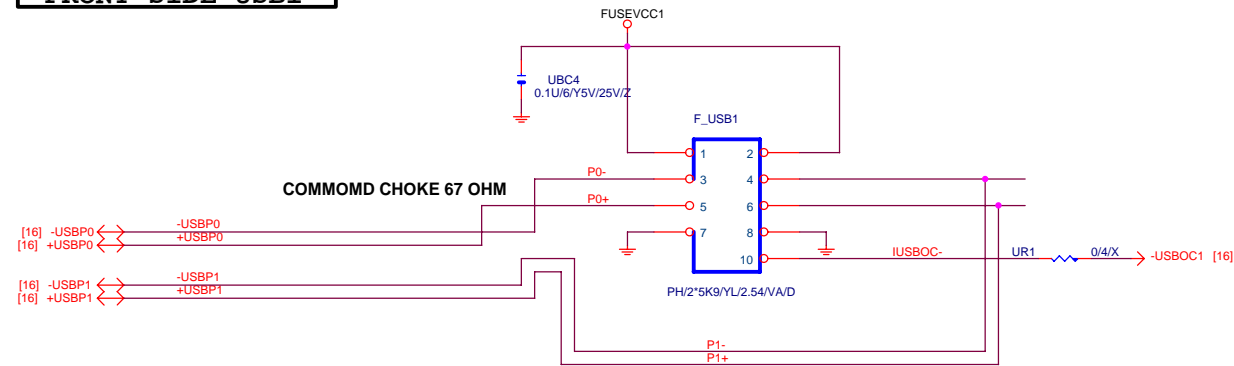
GA-M57SLI-S4

Rev 2.03

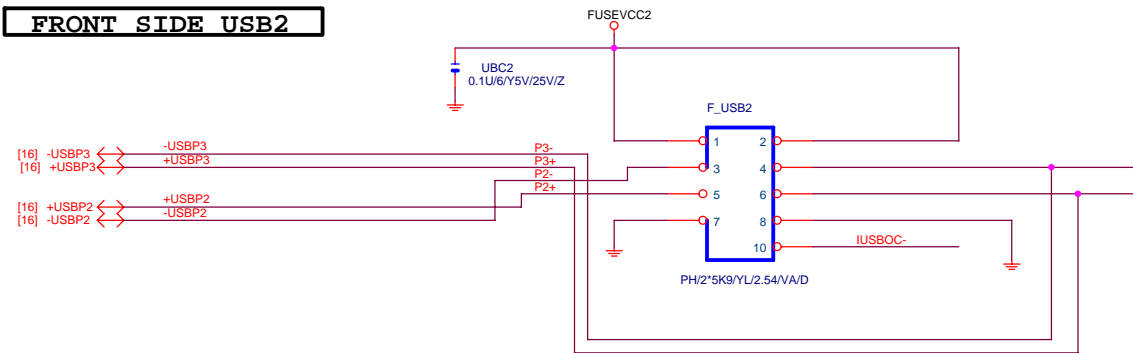
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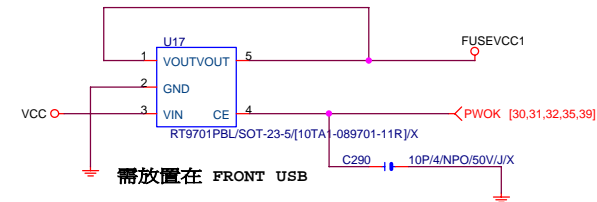
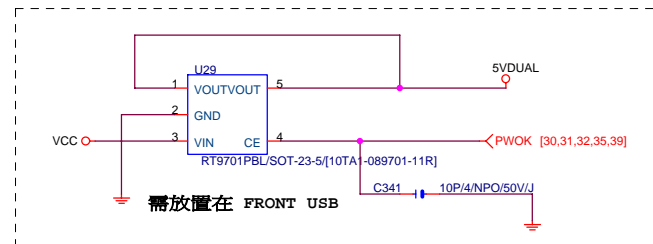
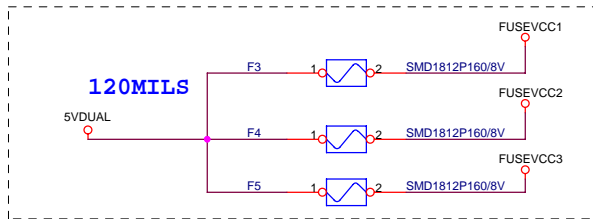
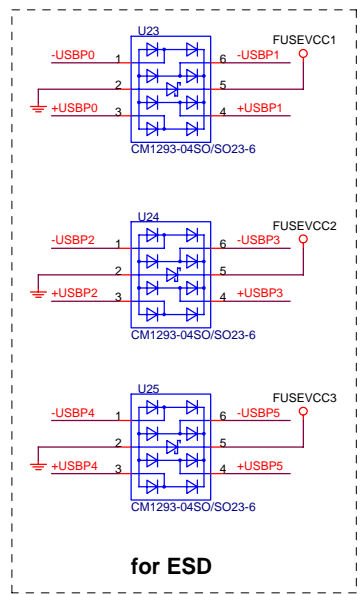
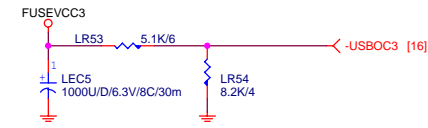
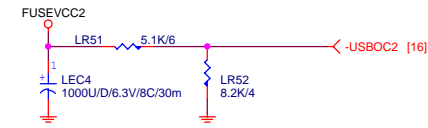
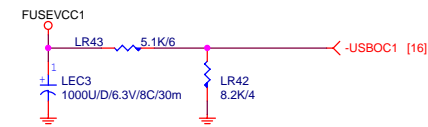
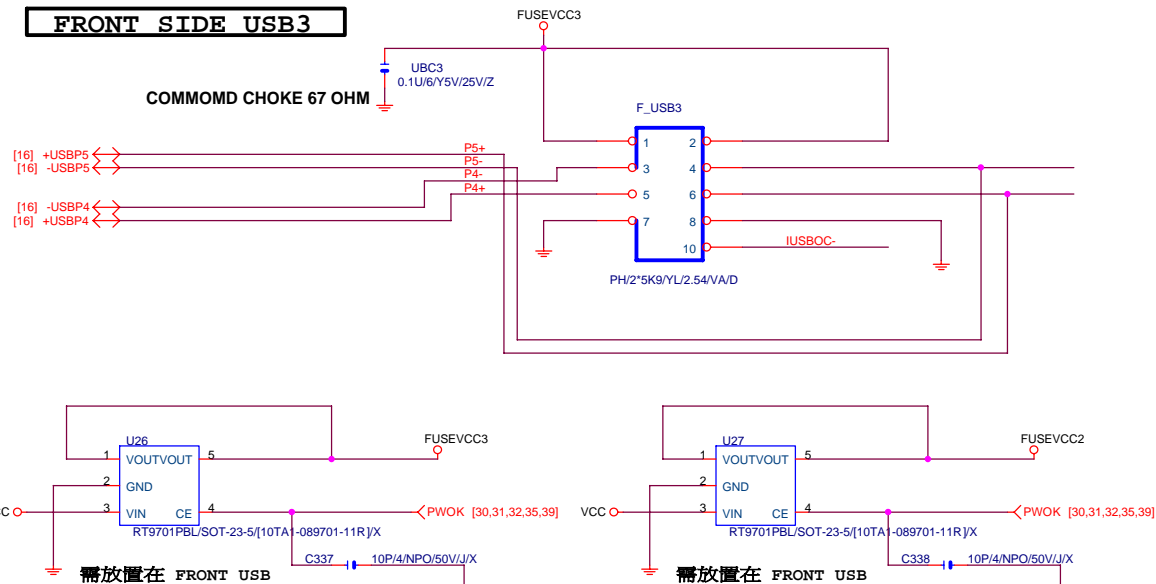
FRONT SIDE USB1



FRONT SIDE USB2



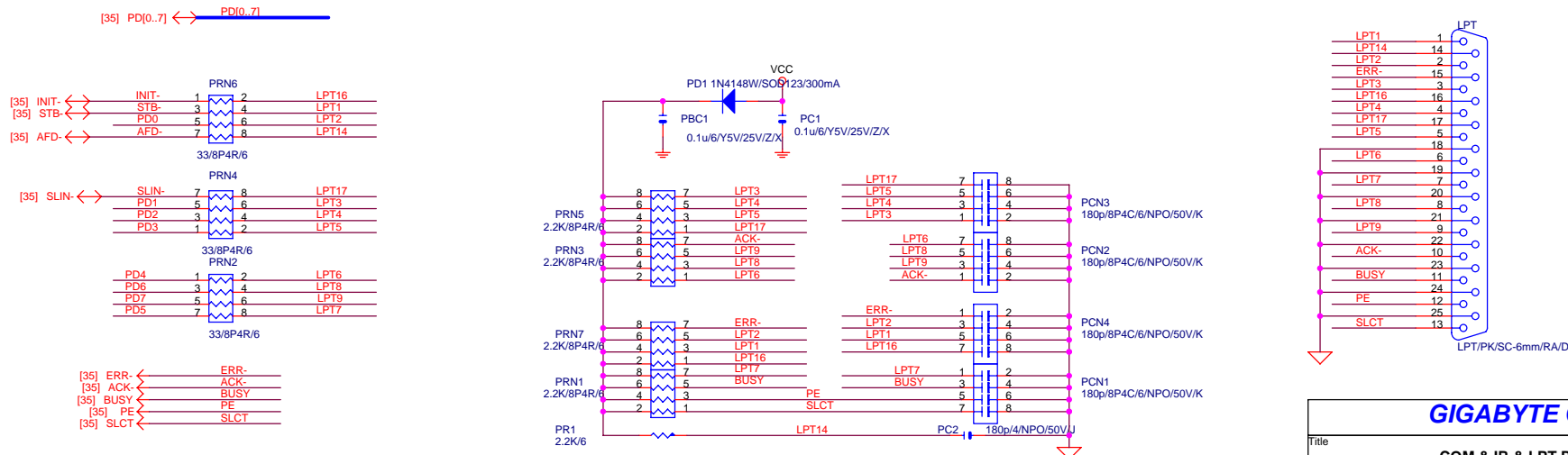
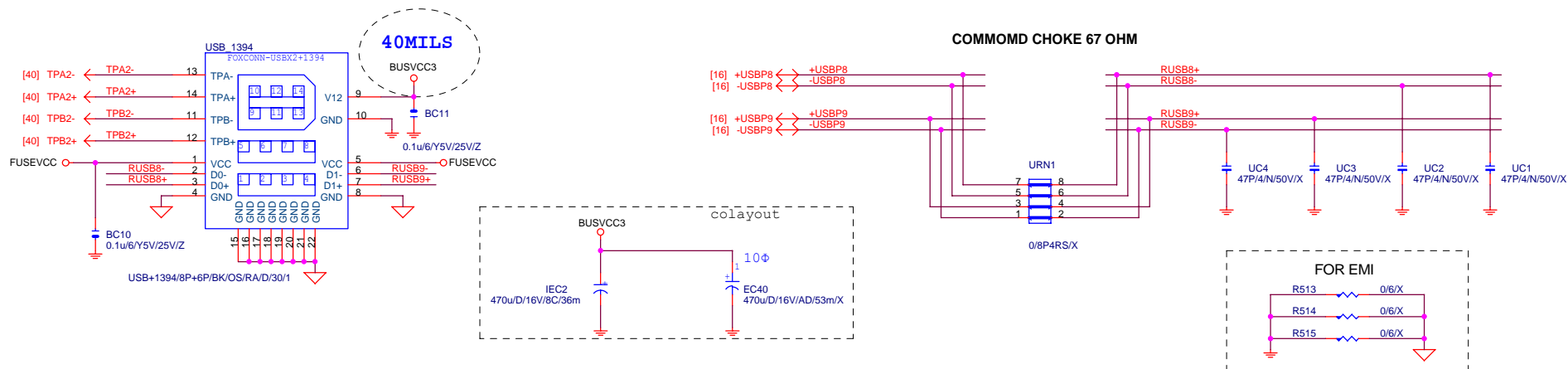
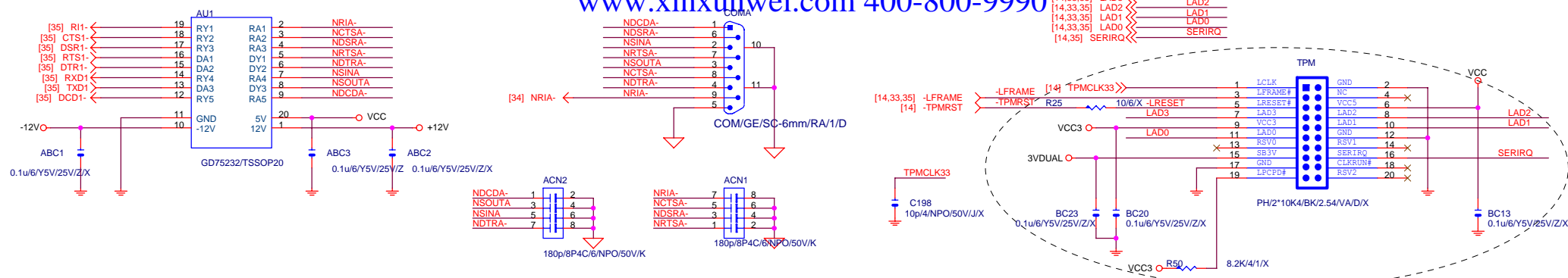
FRONT SIDE USB3



GIGABYTE CORP.

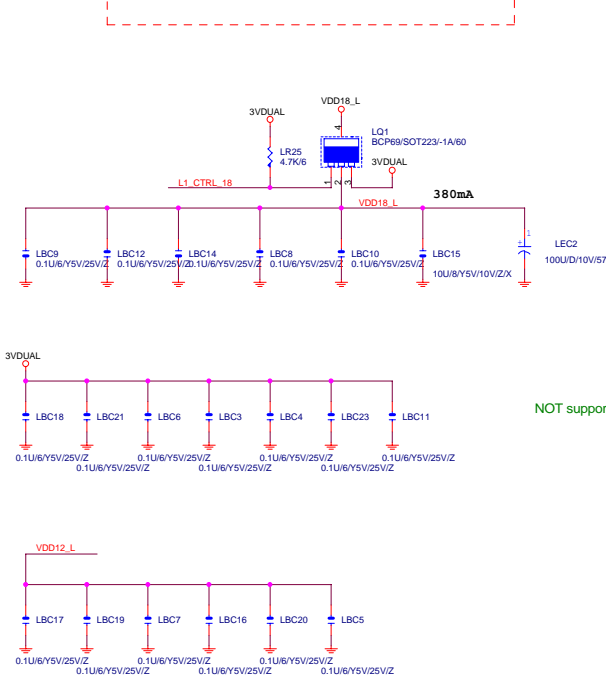
Title			USB PORT
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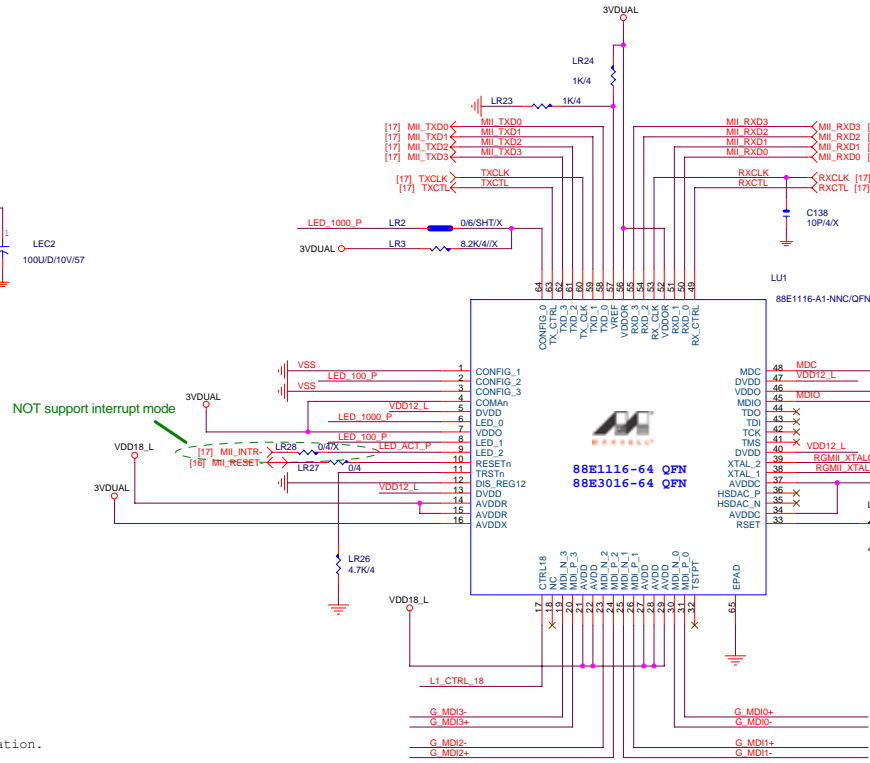
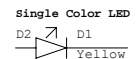
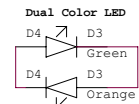
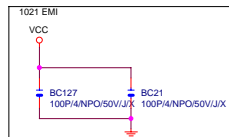
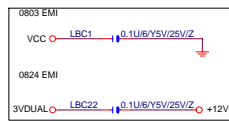


El1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.

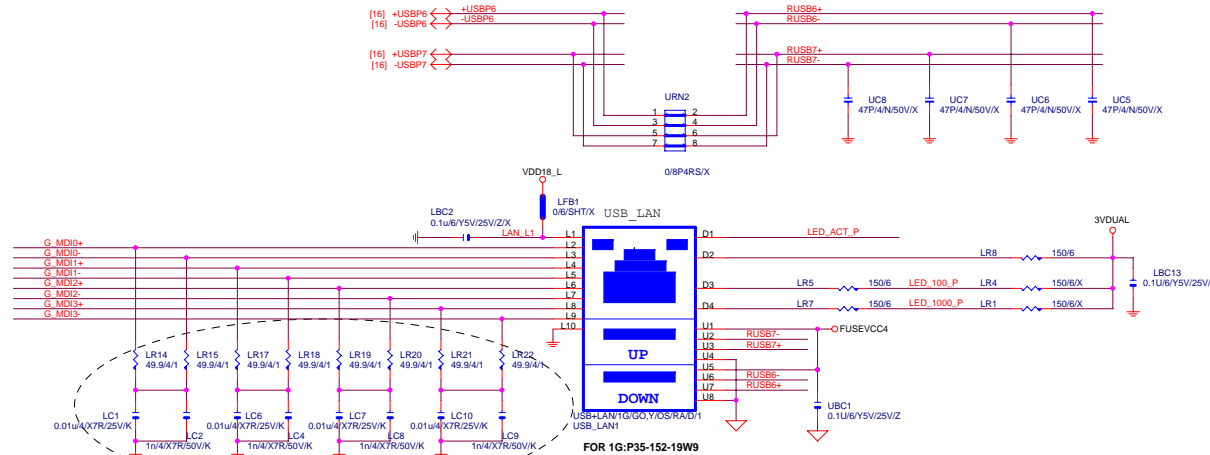
1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities



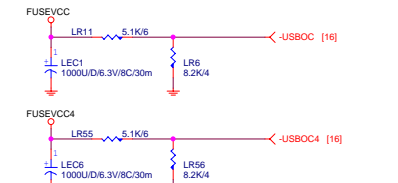
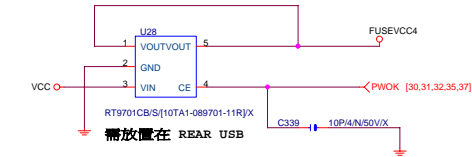
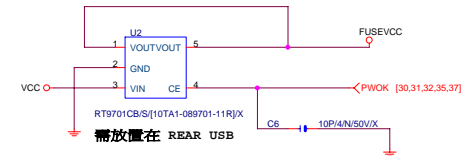
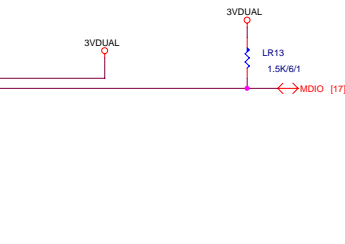
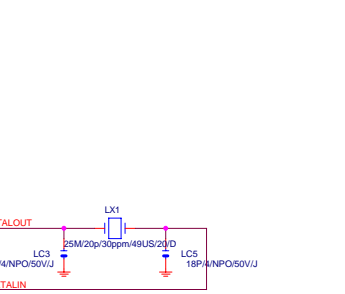
Bypass cap can share. User check it by layout consideration.



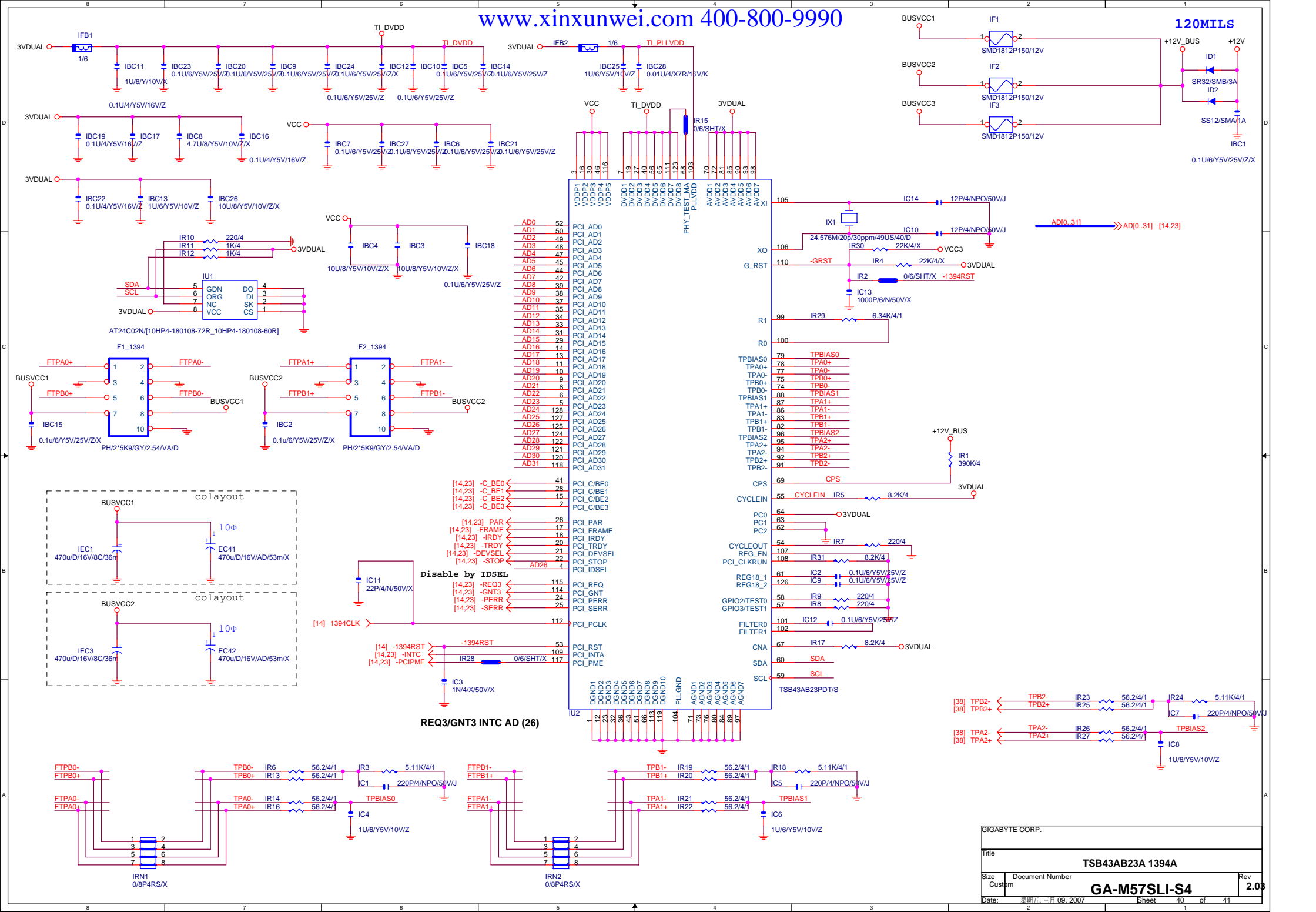
COMMOMD CHOKE 67 OHM

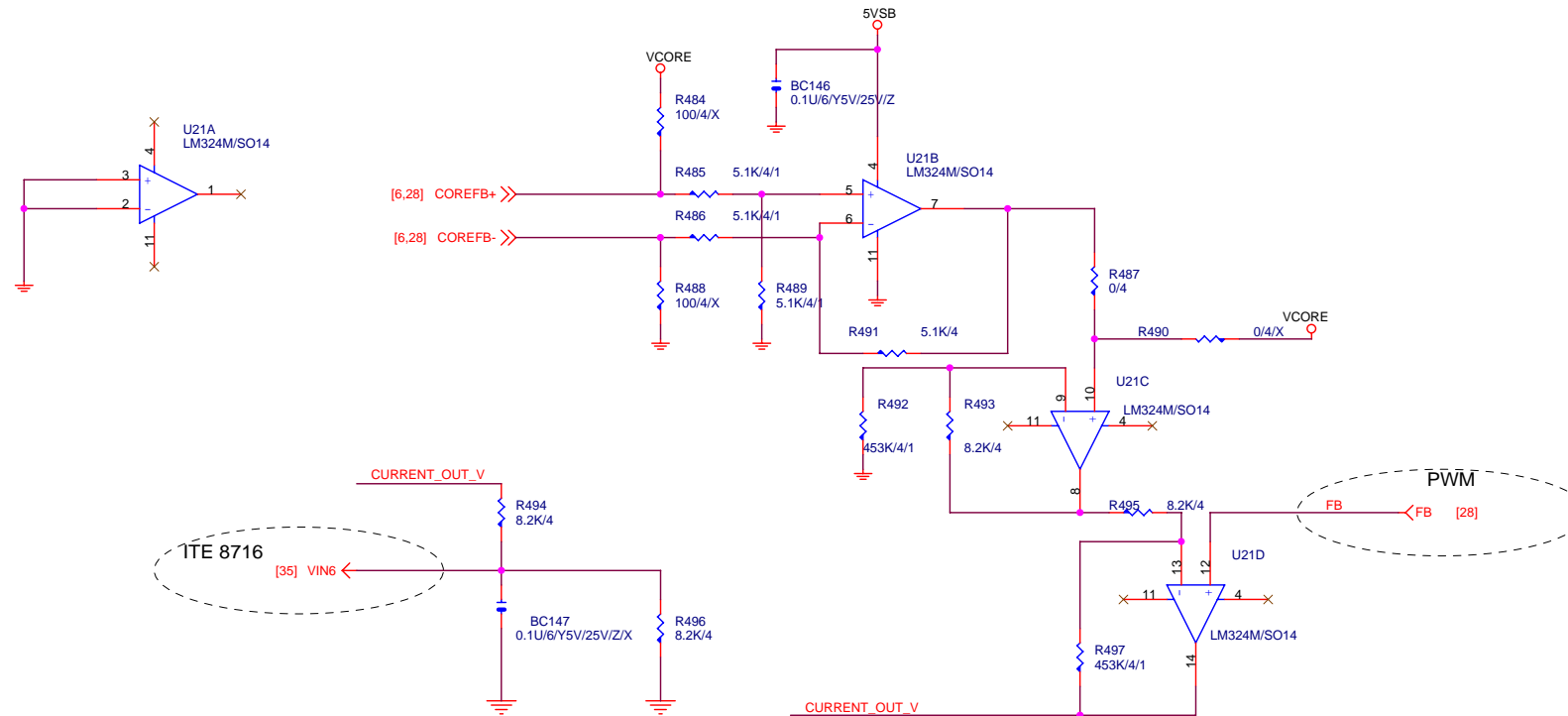


FOR 1G:P35-152-19W9



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